Computer Exercises Manual: Device Parameters in SPICE

A Supplement to
Understanding Semiconductor Devices

Sima Dimitrijev
Griffith University

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SPICE simulator is widely used for computer-aided design of electronic circuits. It enables a variety of very useful analyzes, like frequency response, DC sweep, transient analysis, etc. However, the precision of these analyzes ultimately depends on how well the mathematical models of the semiconductor devices match the real device characteristics. There is a number of device parameters, described in the textbook, whose values should be properly set so that the needed precision of the simulations is achieved. Obviously, there is a need to clearly understand the meaning, and in particular the effects of the most important device parameters. While almost any SPICE manual and many circuit books list the device parameters, they do not explain them; it is assumed that the students and engineers know these parameters.

This manual describes computer exercises that illustrate the effects and the meaning of the device parameters. The exercises are based on circuit simulations\(^1\) involving the basic application circuits that are used to introduce particular devices in the textbook. In this way, the device theory is linked to SPICE as a practical tool for circuit analysis and design. The manual provides complete solutions of all the exercises, presented in the form of figures that include circuit-response diagrams, circuit schematics, and device-parameter values. This format enables a quick and efficient insight into the effects of particular device parameters. The figures are accompanied by detailed descriptions/comments, printed in blue to distinguish them from the introductory text and SPICE instructions (printed in black).

The exercises themselves are relevant for almost any version of SPICE. This is because the device models are common for most of the existing SPICE versions, and therefore the meanings of the device parameters are the same (note that there may be slight differences in notation and default values). For those who are not familiar with SPICE, Section 1 provides a brief description of the SPICE program. Knowledge of SPICE is not a prerequisite – appropriately inserted instructions describe the needed techniques as they are being used. In this case, however, a MicroSim PSPICE v.5 or higher, or OrCAD PSPICE v.9 should be used. The circuit schematic files and the corresponding library files are provided in the “spice” folder (directory) of this CD: the files for the MicroSim version of PSPICE appear in the “MicroSim" subdirectory/subfolder, whereas the files for the OrCAD version of PSPICE appear in the “OrCAD" subdirectory/subfolder.

\(^1\)The exercises in this manual focus on the effects of device parameters on basic circuits. The Interactive MATLAB Animations can be used to plot device characteristics for arbitrary sets of SPICE parameters.
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SPICE BASICS

SPICE\textsuperscript{1} appears as a world-wide standard for computer simulation of electronic circuits. It was originally developed at the University of California, Berkeley, during the mid-1970s. The software is “in the public domain”, meaning that it can freely be used. The original SPICE includes mathematical models of the electrical components/devices and numerical routines for solving electrical circuits. It operates through an input text file that consists of three main parts: (1) component statements (also called circuit description or schematics netlist), (2) analysis setup and (3) semiconductor-device model statements, in addition to a title line\textsuperscript{2}, comment statements, output requests and an end statement.

Nowadays, there are many commercially available and supported versions of SPICE that mostly use the original SPICE core. These products offer many additions and improvements, like extended simulation capabilities and result interpretation. A specifically popular addition is a shell that enables the circuits to be drawn rather than specified by a text file. This shell converts the user’s drawing, as well as menu-selected commands, into appropriate text file that the SPICE core can accept and process. The U.C. Berkeley format of the text input file is retained in almost any commercial version of SPICE.

A particularly popular version of SPICE is PSPICE from MicroSim Corporation, especially its student (evaluation) version that is also freely available. The computer exercises and the circuit schematics (*.sch files), provided in this book, are created using a student version of PSPICE. The circuit diagrams are always shown along with the three main components of the corresponding text input file: Schematic Netlist, the Analysis Setup command, and the Semiconductor Device Model parameters. The text files are shown with every exercise for two important reasons: (1) \textit{generality} – this type of text input file is used by any version of SPICE; (2) all the input numerical values can be seen.

This section describes the syntax of the text input file, and provides references to important SPICE-related information given in the textbook and this manual.

1.1 Schematics Netlist

To prepare or visualize a circuit described by a SPICE text file, all the circuit components and the circuit nodes have to be labeled according to the following rules: (1) the first character of a component label uniquely specifies the type of component, according to Table 1.1, (2) the remaining characters of a component label are arbitrarily selected to uniquely label each individual

\textsuperscript{1}SPICE is an acronym for “Simulation Program with Integrated Circuit Emphasis”.

\textsuperscript{2}The first line of the input file is treated as a title and is ignored by SPICE routines.
component, (3) the nodes are labeled by numbers, where 0 specifies the voltage reference level (circuit “ground”) and must be specified.

Table 1.1 Component labels

<table>
<thead>
<tr>
<th>1st CHARACTER</th>
<th>COMPONENT TYPE</th>
<th>1st CHARACTER</th>
<th>COMPONENT TYPE</th>
</tr>
</thead>
<tbody>
<tr>
<td>B</td>
<td>GaAs MESFET</td>
<td>J</td>
<td>Junction FET</td>
</tr>
<tr>
<td>C</td>
<td>Capacitor</td>
<td>K</td>
<td>Inductor Coupling (Transformer Core)</td>
</tr>
<tr>
<td>D</td>
<td>Diode</td>
<td></td>
<td></td>
</tr>
<tr>
<td>E</td>
<td>Voltage-Controlled</td>
<td>L</td>
<td>Inductor</td>
</tr>
<tr>
<td></td>
<td>Voltage Source</td>
<td>M</td>
<td>MOSFET</td>
</tr>
<tr>
<td>F</td>
<td>Current-Controlled</td>
<td>Q</td>
<td>Bipolar Transistor</td>
</tr>
<tr>
<td>G</td>
<td>Voltage-Controlled</td>
<td>S</td>
<td>Voltage-Controlled Switch</td>
</tr>
<tr>
<td></td>
<td>Current Source</td>
<td>T</td>
<td>Transmission Line</td>
</tr>
<tr>
<td>H</td>
<td>Current-Controlled</td>
<td>V</td>
<td>Independent Voltage Source</td>
</tr>
<tr>
<td></td>
<td>Current Source</td>
<td>W</td>
<td>Current-Controlled Switch</td>
</tr>
</tbody>
</table>

The basic syntax of a line describing a circuit component is

\[
<\text{name}><\text{node}><\text{node}>...\{<\text{value}> \text{ or } <\text{model name}>\}
\]

For example,

\[
\text{R1 1 0 100}
\]

specifies that a 100\(\Omega\) resistor, labeled R1, is connected between the nodes 1 and 0. An additional line like C1 1 0 5p would mean that a capacitor is connected in parallel with the resistor. The capacitor value is expressed as 5p, which is equivalent to \(5\times10^{-12}F = 5pF\). Table 1.2 shows the alphabetic characters, and their numeric equivalents, that can be used immediately after the numeric value as a convenient alternative of expressing large and small numbers. The alphabetic characters shown in Table 1.2 can be followed by more alphanumeric characters, but SPICE will ignore them.

The \(<\text{node}>\) order in the component syntax line is important, as that is how the specific terminals of the devices that are not symmetrical are defined. The SPICE definitions for the devices appearing in this book are given in Table 1.3. For example,

\[
\text{M1 1 2 0 0 IRF}
\]

means that a MOSFET is connected in the following way: the drain to node 1, the gate to node 2, and the source and bulk to node 0 (ground). The last item (the word IRF) means that the characteristics of this MOSFET are specified under the model name IRF. The syntax of device model command is described later.

1.2 Analysis Setup

A number of different types of circuit analyzes can be performed by SPICE. Table 1.4 summarizes those that are used in this book.
Table 1.2 Alphabetic value suffixes

<table>
<thead>
<tr>
<th>SUFFIX</th>
<th>MEANING</th>
<th>NUMERIC</th>
</tr>
</thead>
<tbody>
<tr>
<td>f</td>
<td>femto</td>
<td>$10^{-15}$</td>
</tr>
<tr>
<td>p</td>
<td>pico</td>
<td>$10^{-12}$</td>
</tr>
<tr>
<td>n</td>
<td>nano</td>
<td>$10^{-9}$</td>
</tr>
<tr>
<td>u</td>
<td>micro</td>
<td>$10^{-6}$</td>
</tr>
<tr>
<td>m</td>
<td>milli</td>
<td>$10^{-3}$</td>
</tr>
<tr>
<td>k</td>
<td>kilo</td>
<td>$10^{+3}$</td>
</tr>
<tr>
<td>MEG</td>
<td>mega</td>
<td>$10^{+6}$</td>
</tr>
<tr>
<td>G</td>
<td>giga</td>
<td>$10^{+9}$</td>
</tr>
<tr>
<td>T</td>
<td>tera</td>
<td>$10^{+12}$</td>
</tr>
</tbody>
</table>

Table 1.3 Device terminal definition

<table>
<thead>
<tr>
<th>COMPONENT</th>
<th>NAME</th>
<th>LABEL</th>
<th>1st</th>
<th>2nd</th>
<th>3rd</th>
<th>4th</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resistor</td>
<td>R&lt;name&gt;</td>
<td>&lt;+node&gt;</td>
<td>&lt;+node&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Capacitor</td>
<td>C&lt;name&gt;</td>
<td>&lt;+node&gt;</td>
<td>&lt;+node&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Diode</td>
<td>D&lt;name&gt;</td>
<td>&lt;anode&gt;</td>
<td>&lt;cathode&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MOSFET</td>
<td>M&lt;name&gt;</td>
<td>&lt;drain&gt;</td>
<td>&lt;gate&gt;</td>
<td>&lt;source&gt;</td>
<td>&lt;bulk&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>BJT</td>
<td>Q&lt;name&gt;</td>
<td>&lt;collector&gt;</td>
<td>&lt;base&gt;</td>
<td>&lt;emitter&gt;</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>JFET</td>
<td>J&lt;name&gt;</td>
<td>&lt;drain&gt;</td>
<td>&lt;gate&gt;</td>
<td>&lt;source&gt;</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GaAs MESFET</td>
<td>B&lt;name&gt;</td>
<td>&lt;drain&gt;</td>
<td>&lt;gate&gt;</td>
<td></td>
<td>&lt;source&gt;</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Voltage and current sources, as circuit components, are part of the Schematic Netlist, and have the general syntax described in the previous section. There are, however, details and options that are specifically related to the type of analysis used. The following voltage/current-source description is satisfactory for a .DC or .AC analysis.

<name> <node> <node> DC <value> .AC <magnitude value> <phase value>

Table 1.4 Types of analyzes

<table>
<thead>
<tr>
<th>INPUT-FILE COMMAND LINE</th>
<th>DESCRIBED IN SECTION</th>
<th>COMMENT</th>
</tr>
</thead>
<tbody>
<tr>
<td>.DC &lt;sweep type&gt; &lt;source name&gt;</td>
<td>2.5</td>
<td>DC voltage sweep</td>
</tr>
<tr>
<td>&lt;start value&gt; &lt;end value&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>&lt;step&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>7.1</td>
<td>Component value sweep</td>
</tr>
<tr>
<td></td>
<td>3.7</td>
<td>Temperature sweep</td>
</tr>
<tr>
<td></td>
<td>4.2</td>
<td>Nested sweep</td>
</tr>
<tr>
<td>.AC &lt;sweep type&gt; &lt;number of points&gt;</td>
<td>2.2</td>
<td>Frequency sweep (response)</td>
</tr>
<tr>
<td>&lt;start value&gt; &lt;end value&gt;</td>
<td></td>
<td>(sinusoidal signal assumed)</td>
</tr>
<tr>
<td>.TRAN &lt;print interval&gt; &lt;final time&gt;</td>
<td>2.1</td>
<td>Time response</td>
</tr>
</tbody>
</table>
The DC and AC values are optional. For example,

```
Vin 1 0 DC 5
```

describes a 5V DC voltage source connected between nodes 1 and 0. Similarly,

```
Vin 1 0 AC 5
```

expresses a sinusoidal voltage source with peak magnitude of 5V, zero phase and zero DC voltage (offset). The statement `Vin 1 0 DC 5 AC 5` defines a 5V sinusoidal voltage oscillating around 5V DC offset level. The DC voltage stated in the voltage/current source description is used for the calculation of the circuit operating point, which is always performed before any other analysis. This value becomes irrelevant when the particular source is selected for a DC sweep, as the parameters of the corresponding .DC command line set the DC values to be used during the DC sweep. In the case of AC analysis, the parameters of the corresponding .AC command line set the frequencies of the sinusoidal signal, while the peak amplitude is specified in the AC part of the source description.

In the case of .TRAN analysis, a specific class of input sources has to be used. There are several options, like exponential waveform, pulse waveform, piecewise linear waveform, sinusoidal wave, etc., however, only pulse and sinusoidal waveforms are used in this manual. A pulse waveform is specified in the following way:

```
<name> <node> <node> PULSE(<initial voltage> <pulsed voltage> <delay time> <rise time> <fall time> <pulse width> <period>)
```

For example,

```
Vin 1 0 PULSE(0 5 0 10ns 10ns 0.5us 1us)
```

A sinusoidal wave is specified as follows:

```
<name> <node> <node> SIN(<offset voltage> <peak amplitude> <frequency> <delay> <dumping factor> <phase>)
```

The last three parameters are optional.

### 1.3 Semiconductor Device Models

Let us have a look at the following example:

```
R1 1 0 10k
D1 1 0 BLUE
```

These two lines of a circuit schematics netlist tell us that a resistor of 10kΩ is connected in parallel with a diode. The diode is a non-linear element, and cannot be specified by a single number like 10k in the case of the resistor. The word `BLUE` is an arbitrarily selected `<model name>`, but it means nothing to SPICE unless it is accompanied by appropriate model definition. The syntax of a line defining a device model is:

```
.MODEL <model name> <device type> (<parameter keyword>=<value> <parameter keyword>=<value> ...)
```

As mentioned, `<model name>` is an arbitrary label used by the user, while `<device type>` and `<parameter keyword>` are SPICE words with specific meanings described in Table 1.5. An example of .MODEL statement is:
Table 1.5 The components of .MODEL statement

<table>
<thead>
<tr>
<th>DEVICE DESCRIPTION</th>
<th>MATHEMATICAL MODEL</th>
<th>TEXTBOOK SECTION</th>
<th>TABLES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Diode</td>
<td>D</td>
<td>3.2</td>
<td>A.1, A.2, A.3</td>
</tr>
<tr>
<td>N-channel MOSFET</td>
<td>NMOS</td>
<td>5.4.1</td>
<td>A.4, A.5, A.6, A.7, A.8</td>
</tr>
<tr>
<td>P-channel MOSFET</td>
<td>PMOS</td>
<td>5.4.1</td>
<td>A.4, A.5, A.6, A.7, A.8</td>
</tr>
<tr>
<td>NPN BJT</td>
<td>NPN</td>
<td>6.4.1</td>
<td>A.9, A.10, A.11</td>
</tr>
<tr>
<td>PNP BJT</td>
<td>PNP</td>
<td>6.4.1</td>
<td>A.9, A.10, A.11</td>
</tr>
<tr>
<td>N-channel JFET</td>
<td>NJF</td>
<td>9.2.3</td>
<td></td>
</tr>
<tr>
<td>P-channel JFET</td>
<td>PJF</td>
<td>9.2.3</td>
<td></td>
</tr>
<tr>
<td>N-channel GaAs MESFET</td>
<td>GASFET</td>
<td>9.3.3</td>
<td></td>
</tr>
</tbody>
</table>

.model BLUE D (Is=1p n=1.4)

which means that diode equations with two specified parameters (Is and n) will be used to calculate the characteristics of the components with <model name>=BLUE. Setting the model parameters in PSPICE is described in Section 2.1.
2
CAPACITORS: REVERSE-BIASED P–N JUNCTION

The P–N junction capacitor does not appear as a specific device in SPICE. SPICE diode model includes all the P–N junction related equations and parameters. Therefore, diodes are used to simulate circuits with P–N junction capacitors.

2.1 Some SPICE Basics and $C_{j0}$ (Transient Analysis)

The PSPICE diagram of the high-pass filter [Fig. 2.2 (a) in the textbook] is shown in Fig. 2.1. The high-pass filter itself consist of the diode $D_1$, playing the capacitor role, and the resistor $R_1$.

Exercise 2.1

(a) Open/prepare the file for the high-pass filter circuit shown in Fig. 2.1.

2.1.1 Voltage Sources

The voltage sources $V_{DC}$ and $v_{ac}$ provide the DC and AC components of the input signal. In this particular exercise, the DC component of the input signal is set to 5V (this can be seen from line 4 of the schematic netlist), while the amplitude and the frequency of the AC signal are 5V and 1MHz, respectively (these are the second and third numbers in line 3 of the schematic netlist). A double click on a voltage source opens corresponding window that is used to set/change these values in PSPICE.

Exercise 2.1

(b) Check the settings of $V_{DC}$, $v_{ac}$ and $R_1$, and if necessary set them as in Fig. 2.1.

2.1.2 Transient Analysis

This exercise uses transient analysis in order to obtain voltage-time (or current-time) diagrams as results of the simulation. The total simulation time is set to 2500ns, as can be seen from the Analysis Setup line. This value can be set/changed in PSPICE by clicks on Analysis and Setup, followed by a double click on Transient, which opens the appropriate window. The first number (25ns) is only a print step, it does not affect the simulation itself. The simulation is initiated by Simulate in the Analysis window.
Some SPICE Basics and Cjo (Transient Analysis)

Cjo

* Schematics Netlist *
D.D1 $N_0001 $N_0002 Dbreak
V.vac $N_0002 $N_0003 +SIN 0V 5V 1MEG 0 0 0
V_VDC $N_0003 0 DC 5V
R.R1 0 $N_0001 10k

* Analysis Setup *
.tran 25ns 2500ns

* Semiconductor Device Model *

- .model Dbreak D (Cjo=0)
- .model Dbreak D (Cjo=15pF M=0)
- .model Dbreak D (Cjo=15nF M=0)

---

Fig. 2.1 Exercise 2.1 (a)-(g)
Exercise 2.1
(c) Enable the transient analysis, and set the total simulation time to 2500 ns. Run the simulation.

2.1.3 SPICE Plots - PROBE
The voltage-time (current-time) diagrams can be seen from PSpice using the PROBE tool after the circuit simulation is completed. Probe Setup in the Analysis window can be used to set PROBE to run automatically after the simulation. Once in PROBE, click Trace and Add to bring the window with all the available voltages and currents. To see the input voltage (the voltage @ node 2 in this particular exercise), select \( V(vac:+) \), and PROBE will plot the voltage-time diagram. A click on Plot, followed by Y Axis Settings..., or X Axis Settings... can be used to change the axes ranges set automatically by PROBE.

Exercise 2.1
(d) Display the input voltage, setting the range of y-axis as in Fig. 2.1 (-5 to 10).

The upper voltage-time diagram of Fig. 2.1 shows the instantaneous input signal that can be seen on the computer screen using the PROBE. More voltage-time (or current-time) traces can be added to the same graph, although it is sometimes more convenient to open new PROBE window by clicking Window and New. Again, PROBE will set the axes ranges automatically, that may need to be changed to more conveniently chosen values.

2.1.4 Default \( C_{jo} \) Value
The frequency of the AC signal is set to a fairly high value (1 MHz), and the high-pass filter would be expected to pass the AC component of the input signal onto the output.

Exercise 2.1
(e) Open a new graph window, and arrange the graphs as in Fig. 2.1. Display the output voltage on the second graph, setting the range of y-axis as for the first graph. Comment the result.

The circles in the lower voltage-time diagram of Fig. 2.1 show the result that should be seen if the range of the voltage axis is properly set, and the default value of \( C_d(0) = C_{jo} \) parameter is used in the simulation. Obviously, this result is not consistent with the function of a high-pass filter. The reason for this result is zero default value of the \( C_d(0) = C_{jo} \) parameter, which results with zero capacitance according to the P-N junction capacitor model given in Table A.2. This clearly demonstrates the importance of parameter understanding, and proper parameter setting for any meaningful and confident simulation analysis.

2.1.5 Setting Model Parameters in SPICE
The parameters of semiconductor device models appear in .model statements of the textual input files. The second word in the .model lines represents the model name given to different semiconductor devices in the circuit. In this exercise, the model name is Dbreak, which is the only diode option in the freely available evaluation version of PSpice. The letter D, following the model
name, shows that the set of diode equations is used to model this particular semiconductor device. The model parameters are listed in brackets at the end of the .model line. To set/change device parameters in PSPICE, the device should be selected (click on the device symbol). Consecutive clicks on Edit, Model and Edit Instance Model will open Model Editor window where the device parameters can be typed at the end of the .model line. Proper keywords should be used, otherwise the program will not accept the input file.

2.1.6 Effects of Cjо

Exercise 2.1

(f) To see the effect of Cjо parameter, set its value to 15pF, run the simulation and get the output voltage on the screen.

The solid line in Fig. 2.1 shows the result. An AC signal, oscillating around zero voltage, appears at the output. We can see that the circuit properly removes the DC component of the input signal. However, a closer inspection of the output signal shows that its amplitude is smaller than the amplitude of the input AC signal. Also, there is a phase shift, as the maxima and minima of the input and output signals do not appear at the same times. These effects are related to the value of the capacitor, whose impedance at 1MHz is $1/(2\pi fC) \approx 10k\Omega$, which is comparable to the resistance of the resistor R1. As a consequence, a significant AC voltage drop is wasted across the capacitor.

Obviously, an increase in the value of Cjо parameter should improve the performance of the high-pass filter.

Exercise 2.1

(g) Set Cjо to 15nF, repeat the simulation and plot the output voltage. Compare the result with the case of Cjо=15pF.

As expected, the reduction of the capacitor impedance by 1000 times results in almost ideal performance of the high-pass filter (the dashed line in Fig. 2.1).

Exercise 2.1

(h) Repeat steps (a)-(g) for the case of low-pass filter shown in Fig. 2.2.

2.2 Cjо (AC Analysis)

2.2.1 AC analysis

It is said that a high-pass filter passes high-frequency and blocks low-frequency signals. A low-pass filter acts oppositely, passing low-frequency and blocking high-frequency signals.

What is a high frequency?
What happens at medium frequencies?

To answer these questions, the amplitude of the output voltage should be plotted in a wide range of frequency values. This type of analysis is referred to as AC analysis in SPICE. Otherwise, output voltage–frequency (or current–frequency) plots are known as frequency response curves.
**Figure 2.2 Exercise 2.1 (h)**

### Analysis Setup

```
* Schematics Netlist *
D_D1 0 $N_0001 Dbreak
V_vac $N_0002 $N_0003
+SIN 0V 5V 1MEG 0 0 0
V_VDC $N_0003 0 DC 5V
R_R1 $N_0001 $N_0002 10k

* Semiconductor Device Model *

... .model Dbreak D (Cjo=0)
... .model Dbreak D (Cjo=15pF M=0)
... .model Dbreak D (Cjo=15nF M=0)
```
The Analysis Setup command sets the frequency values used during the simulation, and the AC values of all voltage/current sources will be set to these frequencies.

The frequency sweep comes in three types: linear, octave and decade. The octave and decade sweeps are logarithmic. There are three numerical values in any .ac command line (like in the example of Fig. 2.3): the first number shows how many frequency point will be used in the frequency range, or per octave/decade, depending on what sweep type is selected. The second and third numbers show the start and end frequency values. In PSPICE, the AC analysis is enabled and the parameters set in an analogous way to the transient analysis: clicks on Analysis and Setup, followed by a double click on AC Sweep opens the appropriate window.

### 2.2.2 High-Pass Filter

**Exercise 2.2**

(a) Open the file of high-pass filter circuit.

(b) Set the parameters of VDC, vac and R1 as shown in the Schematics Netlist (Fig. 2.3).

(c) Enable the AC analysis, and set the analysis parameters as in Fig. 2.3: decade sweep, frequency range 10Hz to 10 MHz, and 20 frequency points per decade.

(d) Set CJo value to 0.

(e) Run the simulation and plot the output voltage.

(f) Repeat step (e) for CJo=15pF and CJo=15nF. Set m to 0 in both cases.

(g) Compare and comment the results.

The results of the AC analysis applied to the high-pass filter circuit are given in Fig. 2.3. Obviously, the results depend significantly on the value of CJo parameter. The default value (CJo=0) sets the diode capacitance to zero (an open circuit between the output and the input), which results with zero output voltage at any frequency. The frequency at which the output voltage becomes equal to the input voltage (the whole amount of the input voltage passed through the filter) depends on the capacitance value, as the dashed and solid lines in Fig. 2.3 illustrate. This figure also shows that there is a frequency range where the signal is neither completely passed nor completely blocked.

### 2.2.3 Low-Pass Filter

**Exercise 2.2**

(h) Repeat steps (a)-(g) for the case of low-pass filter shown in Fig. 2.4.

### 2.3 M and VJ

The capacitance of reverse-bias P–N junction depends on the voltage applied. In the previous exercises, this dependence was eliminated by setting the grading coefficient M to zero (refer to the capacitance–voltage equation in Table A.2). The effect of the parameter M can be seen if the result for M=0 is compared to the result obtained with a non-zero value of M:
Exercise 2.3

(a) Open the file of high-pass filter circuit.
(b) Set the parameters of VDC and vac voltage sources as shown in the Schematics Netlist (Fig. 2.3).
(c) Enable the transient analysis, and set the analysis parameters as in Fig. 2.3.
(d) Set the diode parameters as follows: Cjo=15pF, m=0.
(e) Run the simulation and plot the output voltage.
(f) Repeat step (e) for m=0.42 and Vj=0.75.
(g) Compare and comment the results.
The amplitude of the AC signal used in this exercise is large and the instantaneous reverse-bias voltage varies significantly. According to the capacitance–voltage equation of Table A.2, the capacitance in the circuit is different at different instants of time when \( M \neq 0 \). This causes signal distortion, so that the output signal does not have the sine form of the input signal. Note that the distortion does not happen when \( M = 0 \), as the capacitance is constant in this case. Although the
**CAPACITORS: REVERSE-BIASED P–N JUNCTION**

M and $V_J$

---

* Schematics Netlist *

$$D_{D1} \text{ $N_{0001}$ $N_{0002}$ Dbreak}$$

$$V_{\text{vac}} $N_{0002}$ $N_{0003}$$

$$+\text{SIN} 0V 5V 1\text{MEG} 0 0 0$$

$$V_{\text{VDC}} $N_{0003}$ 0 DC 5V$$

$$R_R1 0 $N_{0001} 10k$$

* Analysis Setup *

.$$\text{.tran 25ns 2500ns}$$

* Semiconductor Device Model *

$$\text{.model Dbreak D (Cjo=15pF M=0)}$$

$$\text{.model Dbreak D (Cjo=15pF}$$

$$+M=0.42 \text{ VJ=0.75V)}$$

---

![Diagram](hpfsch.png)

*Fig. 2.5 Exercise 2.3*
M parameter is in the range of $\frac{1}{3}$ to $\frac{1}{7}$, which means it is never 0 in the case of real P–N junctions, the next exercise illustrates that P–N junction capacitors are still very useful components.

2.4 The Effect of Reverse DC Bias

Because of the signal distortion, the P–N junction capacitors are rarely used with large signals. The distortion can be negligible in the case of small signals, as the instantaneous voltage across the P–N junction does not change significantly, and the capacitance remains approximately constant.

Exercise 2.4

(a) Set the parameters of $V_{DC}$ and $V_{AC}$ voltage sources as shown in (Fig. 2.6). The amplitude of the signal is reduced from 5V to 200mV, which can be considered as a small signal. The DC voltage level is set to a small but non-zero value 0.5, ensuring that the instantaneous voltage remains negative (reverse bias) at all times.

(b) Check/set the transient analysis parameters and the diode parameters.

(c) Run the simulation and plot the output voltage.

The result (the dashed line in Fig. 2.6) shows almost sine output voltage. It may be confusing that the first period of the output voltage appears as different and distorted. This is because of the fact that zero voltage and current values, set in the circuit at the beginning of the first period, are different from the voltage and current values that will appear at the beginning of subsequent repeating periods of the signal.

As mentioned earlier, the capacitance changes when the reverse-bias voltage value is changed (the capacitance-voltage equation of Table A.2). This effect can be used to vary the capacitance, and therefore the amplitude of the output voltage, by varying the value of $V_{DC}$ voltage source:

Exercise 2.4

(d) Record the amplitude of the output signal, obtained in point (c).

(e) Change the value of $V_{DC}$ voltage source to 9.5V

(f) Run the simulation and plot the output voltage.

(g) Compare the new amplitude to the one obtained with $V_{DC}=0.5V$ and comment the result.

The solid line of Fig. 2.6 shows that the amplitude of the output signal is smaller for the case of larger DC voltage applied across the P–N junction. This is because an increase in the reverse-bias voltage reduces the depletion-layer capacitance, which in turn means a smaller part of the input voltage is passed on to the output.

The AC analysis, as opposed to the transient analysis, provides better insight into the usefulness of this effect for tuning the frequency response of filters built with P–N junction capacitors.
**CAPACITORS: REVERSE-BIASED P–N JUNCTION**

$M$ and $V_J$

* Schematics Netlist *

\[ \begin{align*}
D_{D1} & : N_{0001} \ N_{0002} \ D_{break} \\
V_{\text{vac}} & : N_{0002} \ N_{0003} \\
+\text{SIN} & : 0V \ 0.2V \ 1\text{MEG} \ 0 \ 0 \ 0 \\
V_{VDC} & : N_{0003} \ 0 \ DC \ 0.5V \\
V_{VDC} & : N_{0003} \ 0 \ DC \ 9.5V \\
R_{R1} & : 0 \ N_{0001} \ 10k \\
\end{align*} \]

* Analysis Setup *

.tran 25ns 2500ns

* Semiconductor Device Model *

.model Dbreak D (Cjo=15pF +M=0.42 VJ=0.75V)

---

**Fig. 2.6** Exercise 2.4 (a)-(g).
Exercise 2.4
(h) Open the file of low-pass filter circuit.
(i) Set the parameters of $v_o$ voltage source as shown in Fig. 2.7, and set the value of $V_{DC}$ to 0.5V.
(j) Enable the AC analysis, and set the analysis parameters as in Fig. 2.7.
(k) Set the diode parameters to $C_{JO}=15pF$, $M=0.42$, and $V_J=0.75$.
(l) Run the simulation and plot the output voltage.
(m) Repeat step (l) for $V_{DC}=9.5V$.
(n) Compare and comment the results.

2.5 The Effect of Forward DC Bias

It has been emphasized several times that P–N junctions can be used as capacitors only with reverse bias. Let us see the results of SPICE simulations for the case of forward bias.

Exercise 2.5
(a) Open the file of low-pass filter circuit.
(b) Set the parameters of $v_o$ voltage source as in Fig. 2.8, and set $V_{DC}$ to 9.5V (reverse bias first).
(c) Enable the transient analysis, and set the analysis parameters as in Fig. 2.8.
(d) Check/set the diode parameters as follows: $C_{JO}=15pF$, $M=0.42$, $V_J=0.75V$.
(e) Run the simulation and plot the output voltage.
(f) Repeat step (e) for $V_{DC}=-9.5V$ (forward bias).
(g) Compare and comment the results.

As the dashed line of Fig. 2.8 shows, the SPICE simulation does give different result for the case of forward-biased P–N junction. The constant output voltage of about $-0.7V$ is not the response that should be obtained from the low-pass filter, which means that the SPICE simulation correctly showed that the low-pass filter cannot be used with $V_{DC}=-9.5V$. This should not be surprising, as the use of a diode to represent a P–N junction capacitor automatically activates the complete diode model in SPICE. Diode, and the complete SPICE model of diodes, are described in Chapter 3 of the textbook.

2.5.1 DC Analysis

Finally, let us use this example to introduce an additional type of SPICE analysis. This type of analysis can help us to sweep the $V_{DC}$ voltage in a wide range, and to find the range where the low-pass filter functions properly. DC sweep parameters are set analogously to the AC analysis. In the .DC analysis command line, the first and second numerical values mean the start and end value of the sweep, while the third number shows the step. The sweep values do not depend on the DC value set as a part of the component setting (shown in the Schematics Netlist).
Exercise 2.5

(h) Open the file of low-pass filter circuit.
(i) Set the parameters of VDC and vac voltage sources as in Fig. 2.9.
(j) Enable the DC analysis, and set the analysis parameters as in Fig. 2.9, selecting the VDC source for DC sweeping (this will override the DC value set in step (i) for the purpose of DC analysis).
(k) Check/set the diode parameters.
(l) Run the simulation and plot the output voltage.
(m) Comment the result.
The Effect of Forward DC Bias

Forward DC Bias

* Schematics Netlist *
D D1 0 N_0001 Dbreak
V_vac N_0002 N_0003
+SIN 0V 0.2V 1MEG 0 0 0
V_VDC N_0003 0 DC 9.5V
R R1 N_0001 N_0002 10k

* Analysis Setup *
.tran 25ns 2500ns

* Semiconductor Device Model *
.model Dbreak D (Cjo=15pF +M=0.42 VJ=0.75V)

Fig. 2.8 Exercise 2.5 (a)-(g).
The output voltage plotted in this case is DC voltage, as opposed to the effective AC voltage in the case of AC analysis. The fact that the vac source is connected and the frequency set to 1MHz does not affect the DC simulation that is performed for the DC case (zero frequency). A low-pass filter is expected to pass the whole value of the input DC voltage on to the output. In other words, the output and input DC voltages should be the same, and output–input DC voltage characteristic should be a straight line with the slope of 1V/V. Fig. 2.9 shows that this
is the case for $V_{DC} > -0.5V$. This is the range in which the P–N junction is reverse biased, and the diode behaves as a capacitor, enabling proper operation of the low-pass filter. For the case of $V_{DC} < -0.5V$, the P–N junction is forward biased, and the filter does not function properly.
3 DIODES: FORWARD-BIASED P–N JUNCTION AND METAL–SEMICONDUCTOR CONTACT

The exercises from this section build on the exercises of Section 2, which cover the parameters associated with the depletion-layer capacitance of diodes.

3.1 IS and N
Two fundamental diode parameters are $I_S = IS$ and $n = N$. The single clamp circuit (Fig. 3.3 in the textbook) can be used to illustrate the effects of these parameters.

**Exercise 3.1**

(a) Open/prepare the file of single clamp circuit shown in Fig. 3.1.
(b) Set the parameters of $V_{sin}$ and $R_1$ as shown in Fig. 3.1. Set the DC voltage source $V_{dc}$ to zero (ideally, zero clamping voltage).
(c) Enable the transient analysis, and set the analysis parameters as in Fig. 3.1.
(d) Set the diode parameters as follows: $I_S = 10^{-14}A$ and $n = 1$.
(e) Run the simulation and plot the output voltage. Record the clamped value of the voltage.
(f) Change $I_S$ to $10^{-10}A$, run the simulation, plot the output voltage, and compare the clamped value of the voltage to the case of $I_S = 10^{-14}A$. Comment the results.

The basic idea of the parameter $I_S$ is that it directly represents the reverse-bias current of the diode. While this is undeniably true, the effect of $I_S$ in the reverse-bias region is nowhere near as important as its effect in the forward-bias region.

The circles and the solid line in Fig. 3.1 show that the negative values of the output voltage (the diode is reverse biased) do not change when the saturation current $I_S$ is increased 10,000 times. Theoretically, the increase in $I_S$ has to change the output voltage, as it changes the voltage drop across the resistor $R_1$. Moreover, it will increase it 10,000 times, however, from $10^{-14} \times 10^3 = 10^{-11}V$ to $10^{-7}V!$ Obviously, this difference is negligible.

Importantly, the saturation current $I_S$ significantly changes the forward-bias voltage of a diode. As this may seem confusing, it is important to clarify this point. If there is a confusion, it is due to a simplistic understanding of the concept of “turn-on” voltage, for example about 0.7V.
* Schematics Netlist *
D_D1 $N_0001 $N_0002 Dbreak
R_R1 $N_0003 $N_0001 1k
V_Vdc $N_0002 0 DC 0V
V_Vsin $N_0003 0
+SIN 0V 2V 60Hz 0 0 0

* Analysis Setup *
.tran 1ms 40ms

* Semiconductor Device Model *
.model Dbreak D (IS=1e-14A N=1)
.model Dbreak D (IS=1e-10A N=1)
.model Dbreak D (IS=1e-10A N=2)

Fig. 3.1 Exercise 3.1
in the case of silicon diode. The diode does not turn suddenly at a certain “turn-on” voltage, but the current increases exponentially as the forward-bias voltage is increased (refer to the diode model in Table A.1). We consider that a diode is in “on” mode when its current reaches an implicitly set level. The voltage drop across the diode ($V_{D0}$) that corresponds to the set current level depends on $I_S$, which is obvious from the diode model (Table A.1). In the example of the clamp circuit, (Fig. 3.1), the increase in $I_S$ corresponds to a reduction in $V_{D0}$ voltage, therefore to a reduction in the output clamped voltage. Technically speaking, we can say that the “turn-on” voltage of the diode is reduced from about 0.7V to about 0.45V when $I_S$ is increased from $10^{-14}$A to $10^{-10}$A.

**Exercise 3.1**

(g) Change $n$ to 2, and observe the effect on the clamped voltage. Comment the results.

The saturation current $I_S$ is not the only parameter that affects the forward-bias current-voltage characteristic of the diode. The second parameter is the emission coefficient $n$. Practical values of $n$ vary between 1 (pure diffusion current) and 2 (total dominance of either recombination current or high-injection effects). The dashed line in Fig. 3.1 shows that the increase of $n$ from 1 to 2 reduces the diode current so much that the gain in reduced output voltage, achieved by 10,000-fold increase in $I_S$, is more then lost.

As both $I_S$ and $n$ dramatically influence the forward-bias diode characteristic, these parameters should be set in SPICE simultaneously.

### 3.2 Schottky Diode (Turn-On Voltage Versus $I_S$)

As a continuation of the previous exercise, let us compare the use of a P–N junction and Schottky diode in the rectifying circuit (Fig. 3.2 a in the textbook). Schottky diodes exhibit much smaller “turn-on” voltages, which can be advantageous in rectifying circuits. The Schottky diode is simulated in SPICE by the same diode model of Table A.1. As shown in the previous exercise, the parameter $I_S$ can be set to a proper value in order to obtain the smaller “turn-on” voltage of the Schottky diode.

**Exercise 3.2**

(a) Open/prepare the file of rectifier circuit shown in Fig. 3.2.

(b) Set the parameters of $V1$ and $R1$ as in Fig. 3.2.

(c) Enable the transient analysis, and set the analysis parameters as in Fig. 3.2.

(d) Set $I_S$ to $10^{-14}$A and $n$ to 1, to represent a P–N junction diode.

(e) Run the simulation and plot the input and output voltages. Record the values of maximum and minimum output voltages.

(f) Change $I_S$ to $10^{-4}$A, to represent a Schottky diode. Run the simulation, plot the input and output voltages, and compare the maximum and minimum voltages to the case of the P–N junction diode. Comment the results.

As expected, the forward-bias voltage drop across the Schottky diode (the solid line in Fig. 3.2) is so small that the positive output voltage is almost equal to the input voltage. As opposed to this, there is a significant voltage difference in the case of the P–N junction diode (the circles), which is equal to the diode “turn-on” voltage $V_D$.

A closer inspection of the output voltage, corresponding to the negative half-period of the input voltage, indicates that there will be a practical limit to the reduction of the “turn-on”
The saturation current is increased so much in this case ($10^{10}$ times) that the voltage drop across $R_1$ due to the reverse-bias current $I_S$ becomes observable. At this level of $I_S$, the negative voltage is still tolerable. However, an increase in $I_S$ by only a single additional order of magnitude would increase the negative voltage to $10^{-3}A \times 1\,k\Omega = 1V$, which is comparable to the input voltage.

The fact that the same model is used in SPICE for both, P–N junction and Schottky diodes, does not mean that a P–N junction with appropriately designed physical parameters can provide the I-V characteristic of a Schottky diode. It is correct that the saturation current $I_S$ of a P–N junction diode depends on the doping level, and also depends on the P–N junction area. This

---

**Fig. 3.2 Exercise 3.2**
dependencies are given by Eq. (3.15) in the textbook. However, the doping concentrations cannot be reduced by 10 orders of magnitude, to increase the $I_S$ to the level needed to emulate a Schottky diode. Can the P–N junction area be increased so much? Assume that $I_S = 10^{-14}A$ corresponds to a $50\mu m \times 50\mu m$ P–N junction diode. To obtain $I_S = 10^{-4}A$, the needed P–N junction area would be $25m^2$!

### 3.3 $RS$

Let us take again the single-clamp circuit to check the effect of the third diode parameter from Table A.1 - the parasitic resistance $r_S = RS$.

**Exercise 3.3**

(a) Open the file of single clamp circuit.

(b) Check/set the parameters of $V_{sin}$, $V_{dc}$ and $R1$, and the transient analysis parameters as in Fig. 3.3.

(c) Set the diode parameters as follows: $I_S = 0.1pA$, $n = 1$, and $r_S = 0$.

(d) Run the simulation and plot the output voltage. Record the values of maximum output voltage.

(e) Change $r_S$ to $16\Omega$, run the simulation, plot the output voltage, compare and comment the results.

The obtained results, given in Fig. 3.3, show no difference between the simulations with $r_S = 0$ and $r_S = 16\Omega$. Does this mean the effects of $r_S$ can always be neglected?

**Exercise 3.3**

(f) Change the value of the resistor $R1$ to $50\Omega$.

(g) Repeat steps (c), (d) and (e).

Different results are obtained this time, as shown in Fig. 3.4. The difference is due to the fact that the parasitic diode resistance $r_S = 16\Omega$ is comparable to the value of resistor $R1$.

### 3.4 $BV$ and $RS$

The forth static-parameter of the diode (Table A.1) is the breakdown voltage $BV$. The reference-voltage circuit, introduced in Section 3.3.1 of the textbook (Fig. 3.15), can be used to illustrate the effects of this parameter.

**Exercise 3.4**

(a) Open/prepare the file of reference voltage circuit shown in Fig. 3.5.

(b) Set the parameters of $V_{in}$, $R1$ and $R_{load}$ as in Fig. 3.5.

(c) Enable the transient analysis, and set the analysis parameters as in Fig. 3.5.

(d) Set $I_S$ to $10^{-14}A$ and $n$ to 1, but ignore $BV$.

(e) Run the simulation, plot the output voltage and the current flowing through the diode, and comment the results.

The breakdown voltage of a diode can vary in a very wide range, from several volts to thousands of volts. The default value is usually set to infinity ($BV = \infty$). If the breakdown voltage of the diode $D1$ in the circuit of Fig. 3.5 is larger than $V_{in}$, the diode appears as an open circuit (zero diode current), and the circuit is simply a voltage divider. The circles in Fig. 3.5 show that the output voltage directly follows the changes of the input voltage.
RS vs $R_1$

* Schematics Netlist *

D_D1 $N_{0001}$ $N_{0002}$ Dbreak
R_R1 $N_{0003}$ $N_{0001}$ 1k
V_Vdc $N_{0002}$ 0 DC 0V
V_Vsin $N_{0003}$ 0
+SIN 0V 2V 60Hz 0 0 0

* Analysis Setup *

.tran 1ms 40ms

* Semiconductor Device Model *

.model D Dbreak(IS=0.1pA N=1

○ ○ ○ + RS=0)

___ + RS=16)

**Fig. 3.3** Exercise 3.3 (a)-(e).
**DIODES: FORWARD-BIASED P–N JUNCTION AND METAL–SEMICONDUCTOR CONTACT**

**Fig. 3.4** Exercise 3.3 (f)-(g).

---

**RS vs \( R_1 \)**

* Schematics Netlist *

\[
\begin{align*}
D\_D1 & \ $N\_0001$ $N\_0002$ Dbreak \\
R\_R1 & \ $N\_0003$ $N\_0001$ 50 \\
V_{Vdc} & \ $N\_0002$ 0 DC 0V \\
V_{Vsin} & \ $N\_0003$ 0 \\
+& \ SIN 0V 2V 60Hz 0 0 0
\end{align*}
\]

* Analysis Setup *

\[.tran 1ms 40ms\]

* Semiconductor Device Model *

\[.model D Dbreak(IS=0.1pA N=1 RS=0)\]

\[.model D Dbreak(IS=0.1pA N=1 RS=16)\]

---

**TIME (ms)**

**V @ node 1 (V)**

**V @ node 3 (V)**

**V(Vsin:+)**

---
* Schematics Netlist *
D.D1 0 $N.0001 Dbreak
R.R1 $N.0002 $N.0001 100
R.Rload 0 $N.0001 1k
V.Vin $N.0002 0
+SIN 7V 0.5V 60Hz 0 0 0

* Analysis Setup *
.tran 1ms 40ms

* Semiconductor Device Model *
.model Dbreak D (IS=1e-14A N=1)
.model Dbreak D (IS=1e-14A N=1
+ BV=4.7V RS=0)
.model D Dbreak(IS=1e-14A N=1
+ BV=4.7V RS=10)

Fig. 3.5 Exercise 3.4.
Exercise 3.4
(f) Set $BV$ to 4.7V and $RS$ to 0.
(g) Run the simulation, plot the output voltage and the diode current, and comment the results.

As the input voltage is maintained at a higher level than 4.7V, the third line of $I_D(V_{D0})$ equation given in Table A.1 is active during the circuit simulation. This equation models the breakdown region of the diode, where the current sharply rises with any small increase in the reverse-bias voltage. The solid lines in Fig. 3.5 show that hardly observable changes in the output voltage (this is the reverse-bias voltage $-V_{D0}$) produce large enough changes in the diode current to accommodate the input voltage changes. The important result is that a constant voltage level is maintained across the load element $R_{load}$.

Is $r_S$ parameter important for the reference-voltage circuit?

Exercise 3.4
(h) Record/print the results for the case of $r_S = 0$.
(i) Change $r_S$ to 10Ω.
(j) Run the simulation, and plot the output voltage and the diode current. Compare the results to the case of $r_S = 0V$, and comment the differences.

In terms of the effects of $r_S$, this circuit is similar to the single-clamp circuit analyzed in the previous exercise. In both cases, the effects of $r_S$ would not be noticeable if $R1$ was much larger than $r_S$. For the case of $R1 = 10r_S$, the dashed line in Fig. 3.5 shows minor variations in the output voltage.

3.5 $C_{jo}, M$ and $V_J$

Let us consider the performance of a diode in the voltage rectifier circuit (Fig.3.2 a in the textbook) at high frequencies.

Exercise 3.5
(a) Open/prepare the file of rectifier circuit shown in Fig. 3.6.
(b) Set the parameters of $V1$ and $R1$ as in Fig. 3.6.
(c) Enable the transient analysis, and set the analysis parameters as in Fig. 3.6.
(d) Set the diode parameters as follows: $I_S = 0.1pA$, $n = 1$, and $r_S = 16Ω$.
(e) Run the simulation, plot the output voltage, and comment the results.

As the circles in Fig. 3.6 show, it appears the diode works perfectly: the positive voltage is passed to the output as the diode is in “on” mode, while the negative voltage is blocked as the diode is in “off” mode. Should the frequency of the input signal influence the response of the rectifier?

Exercise 3.5
(f) Add the following diode parameters: $C_d(0) = 2pF$, $m = 0.5$, and $V_{bi} = 0.75V$. Note that these parameters are considered in detail in the capacitor related exercises (Section 2).
(g) Run the simulation, plot the output voltage, and comment the results.

The solid line in Fig. 3.6 illustrates the difference that the depletion-layer capacitance makes. This capacitance is too small to make any difference at small frequencies, and the circuit prop-
erly rectifies the input signal. However, as the frequency is increased, the capacitance begins to dominate the diode performance and the circuit increasingly resembles the high-pass filter.

3.6 TT

The depletion-layer capacitance, considered in the previous exercise and the exercises of Section 2, is not the only capacitance component responsible for the dynamic characteristics of a diode. As Table A.2 shows, \( \tau_T = TT \) is an additional dynamic parameter, related to an additional capacitance component referred to as the stored-charge capacitance. The single-clamp circuit can
illustrate the importance of \( \tau_T \) parameter, although much better insight into the meaning of this parameter will be gained from the exercise related to the double-clamp circuit.

### 3.6.1 The Importance of \( \tau_T \) at Different Frequencies: Single Clamp Circuit

**Exercise 3.6**

(a) Open the file of single clamp circuit.
(b) Set the DC voltage source to 6V.
(c) Set the amplitude of the voltage source \( V_{\text{sin}} \) to 15V, and its frequency to 1MHz, as shown by line (a) in Fig. 3.7.
(d) Enable the transient analysis and set the total analysis time to 2500ns, as in line (a) in Fig. 3.7.
(e) Set the diode parameters as follows: \( I_S = 0.1 \mu A \), \( n = 1 \), \( r_S = 16 \Omega \), \( C_d(0) = 2pF \), \( m = 0.5 \), \( V_b = 0.75V \), and \( \tau_T = 0 \).
(f) Run the simulation and plot the input and output voltages. Record/print the results.
(g) Change \( \tau_T \) to 12ns, run the simulation, plot the input and output voltages, compare and comment the results.

As the plots in Fig. 3.7 (a) show, the single-clamp circuit works as expected, clamping the voltages higher than \( V_{dc} = 6V \), and passing the lower voltages without any distortion. This means that neither the depletion-layer capacitance nor the stored-charge capacitance (\( \tau_T \) parameter) has an observable effect at this frequency.

**Exercise 3.6**

(h) Change the frequency of \( V_{\text{sin}} \) to 100MHz, and the total analysis time to 25ns, as shown by lines (b) in Fig. 3.7.
(i) Repeat steps (e), (f) and (g).

The circles in Fig. 3.7 (b) show the effect of the depletion-layer capacitance alone (\( \tau_T = 0 \)). Obviously, the diode in “off” mode does not behave as an open circuit but as a capacitor causing a phase shift and a slight amplitude reduction of the voltage that is meant to be passed without any distortion. However, the solid line shows that the stored-charge capacitance (\( \tau_T = 12ns \)) causes further distortion. It can be seen that the effect of \( \tau_T \) parameter is not symmetrical: there is a difference between the circles and the solid line when the voltage drop across the diode is being reduced, and there is no difference when the voltage drop increases. The reason for this can better be understood by the following analysis, based on the double-clamp circuit shown in Fig. 3.4 of the textbook.
* Schematics Netlist *
D_D1 $N_0001$ $N_0002$ Dbreak
R_R1 $N_0003$ $N_0001$ 1k
V_Vdc $N_0002$ 0 DC 6V
V_Vsin $N_0003$ 0
(a) +SIN 0V 15V 1MEG 0 0 0
(b) +SIN 0V 15V 100MEG 0 0 0

* Analysis Setup *
(a) .tran 50ns 2500ns
(b) .tran 0.5ns 25ns

* Semiconductor Device Model *
.model Dbreak D (IS=0.1pA N=1
+ RS=16 Cjo=2pF M=0.5 VJ=0.75V

Fig. 3.7 Exercise 3.6 (a)-(i)
3.6.2 Understanding TT: Double Clamp Circuit

Exercise 3.6

(j) Open/prepare the file of double clamp circuit, shown in Fig. 3.8.

(k) Set the parameters of $V_+$, $V_-$, Rin, Cgate, and Rgate as in Fig. 3.8.

(l) Set the parameters of the input pulse voltage as in Fig. 3.8: low voltage level $-7V$, high voltage level 100V, rise and fall times 5ns each, pulse width 100ns, and period 200ns. While both the low and the high voltage levels exceed the power supply levels $V_-$ and $V_+$, respectively, the differences are purposefully set to significantly different values: $|−7V|−|−6V| = 1V$, as opposed to $100V−6V = 94V$.

(m) Enable the transient analysis and set the total analysis time to 400ns, as in Fig. 3.8.

(n) Set the diode parameters as follows: $I_s = 0.1pA$, $n = 1$, $r_s = 16\Omega$, $C_d(0) = 2pF$, $m = 0.5$, $V_b = 0.75V$, and $\tau_T = 0$.

(o) Run the simulation and plot the input and output voltages. Record/print the results.

(p) Change $\tau_T$ to 12ns, run the simulation, plot the input and output voltages, compare and comment the results.

The solid and dashed lines in Fig. 3.8 show the output voltage with and without the effect of $\tau_T$, respectively. It is obvious that the effect of $\tau_T$ shows only when the output voltage changes from positive to negative. This behavior is related to the amplitude of the input voltage. When the positive input voltage of 100V is applied to the input, diode D1 is turned “on”, clamping the output voltage (node 2) to a little above $V_+=6V$. The current that flows through the diode is $\approx (100−6)V/1k\Omega = 94mA$. The stored charge is proportional to the current flowing through the diode (Eq. 3.23 in the textbook), the proportionality coefficient being the transit time. When the input voltage changes to negative, this diode cannot turn off before the stored charge is removed from the edges of the depletion layer, causing the observed delay in the fall of the output voltage. This delay depends on the charging and discharging circuits, because it depends on the amount of stored charge (which further depends on the transit time $\tau_T$) and the rate at which the stored charge is being removed.

The fact that it is not the transit time $\tau_T$ alone that determines the turn-off delay time is powerfully illustrated by the case of technologically identical diode D2. This diode is turned when the negative voltage of $−7V$ is applied to the input, as this diode clamps the voltage to $−6V$. However, much less charge is stored at the depletion-layer edges of this diode, as much smaller current flows through it: $< (−6V−(−7V))/1k\Omega = 1mA$. Consequently, it takes much faster to discharge this diode when the positive voltage appears at the input.

3.7 Temperature Analysis

The ambient temperature influences device characteristics, and SPICE can include the temperature effect. Normally, the simulation is performed for $27^\circ C$, however, the temperature can be set to any other value. In PSPICE, this is done by clicks on Analysis, Setup, and Temperature, which opens a window where the desired value of the temperature can be typed in. This results with a .TEMP $<$value$>$ statement in the Analysis Setup input file, where $<$value$>$ is the newly setup temperature value in $^\circ C$. 


Temperature Analysis

* Schematics Netlist *

R_Rin $N_0002 $N_0001 1k
V_V+ $N_0003 0 DC 6
V_Vp $N_0001 0 PULSE -7V 100V
+0 5ns 5ns 100ns 200ns
V_V- 0 $N_0004 DC 6V
D_D1 $N_0002 $N_0003 Dbreak
D_D2 $N_0004 $N_0002 Dbreak
R_Rgate 0 $N_0002 1G
C_Cgate 0 $N_0002 10f

* Analysis Setup *

.tran 4ns 400ns

* Semiconductor Device Model *

.model Dbreak D (IS=0.1pA N=1
+ RS=16 Cjo=2pF M=0.5 VJ=0.75V

+ TT=0ns)

+ TT=12ns)

---

Fig. 3.8 Exercise 3.6 (j)-(p)
3.7.1 DC Analysis - Sweeping the Temperature

In order to study the effect of temperature changes, SPICE allows temperature sweep, very much alike the sweep of DC voltage/current values. To set a temperature sweep in PSPICE, open the DC Sweep window by clicking Analysis, Setup and DC Sweep, then select Temperature and type Start Value, End Value, and Increment. This will result with an Analysis Setup command as in Fig. 3.9, where the start value is $-50^\circ C$, the end value is $100^\circ C$, and the increment is $5^\circ C$.

It is not possible in SPICE to set different components of a circuit at different temperatures. When the temperature setting is changed in either of the above-described ways, any component of the circuit is exposed to the changed temperature. However, many component parameters will not be affected, as they are considered as temperature independent.

As the “turn-on” voltage of P–N junction diodes changes with temperature, a circuit similar to the single-clamp circuit with $V_{dc}=0$ can be used as a temperature sensor.

**Exercise 3.7**

(a) Open the file of single clamp circuit.

(b) Set $V_{dc}$ to $0V$ and check the value of $R_1$.

(c) Although $V_{sin}$ is generally intended as a sinusoidal voltage source, it can be used to produce a DC voltage only. This is achieved by setting the DC voltage level to the desired value ($5V$ in this exercise), and by setting the amplitude of the sinusoidal voltage to $0V$.

(d) Enable the DC Analysis transient, setting Temperature as the sweeping variable, as in Fig. 3.9.

(e) Set the diode parameters as follows: $I_s = 0.1pA$, $n = 1$, and $r_s = 16\Omega$.

(f) Run the simulation and plot the output voltage. Comment the results.

Fig. 3.9 shows the results obtained by this type of analysis. The output voltage of the circuit is basically the “turn-on” voltage of the diode that linearly decreases with increase in temperature. Of course, the output voltage can be amplified and calibrated to display the value of the measured temperature. As the diode is the sensing element, in reality, only the diode may be exposed to the varying temperature. In SPICE, the temperature is varied for all the components in the circuit, and a care should be taken when interpreting the simulation results. In this case, the values of all other components of the circuit are temperature independent, so it does not make any difference.
Temperature Analysis

* Schematics Netlist *
D_D1 $N\_0001 $N\_0002 Dbreak
R_R1 $N\_0003 $N\_0001 1k
V_Vdc $N\_0002 0 DC 0V
V_Vsin $N\_0003 0 DC 5V
+SIM 0V 0V 60Hz 0 0 0

* Analysis Setup *
.DC LIN TEMP -50 100 5

* Semiconductor Device Model *
.model Dbreak D (IS=0.1pA N=1 RS=16)

**Fig. 3.9 Exercise 3.7**
4

MOSFET

Following the conclusions of Section 5.4 in the textbook, LEVEL 3 MOSFET model is used in all the exercises presented in this section. The model selection is by way of setting the LEVEL parameter. Therefore, LEVEL=3 will always appear as the first parameter.

4.1 $V_{to}, K_P, L, \text{and } W$

$L$ and $W$ can be set as either geometrical variables or device parameters. The first option is used in the following exercises. Consequently, $L$ and $W$ values appear in the appropriate device line of the Schematics Netlist. In PSpice, a double click on the MOSFET symbol opens a window where values of the geometrical variables can be typed in.

In addition to $L$ and $W$, two essential MOSFET parameters are $V_{T0}$ and $K_P$. The transfer characteristic of a MOSFET in the linear region illustrates the effects of $V_{T0}$ and $K_P$.

4.1.1 Transfer Characteristic

Exercise 4.1

(a) Open/prepare the file of MOSFET biasing circuit, shown in Fig. 4.1.
(b) Set the channel length and width of the MOSFET to 3$\mu m$ and 100$\mu m$, respectively.
(c) Set $V_{DS}$ to 50$mV$ to ensure that the MOSFET is in the linear region. For a start, set $V_{SB}$ and $V_{GS}$ to zero.
(d) Enable the DC analysis, and set the analysis parameters as in Fig. 4.1.
(e) Set the MOSFET parameters as follows: $V_{T0} = 0V$ and $K_P = 20\mu A/V^2$. These are the usual default values.
(f) Run the simulation and plot the drain current ($ID(M1)$). Record/print the result.
(g) Change $V_{T0}$ to $1V$, run the simulation and plot the drain current. Compare and comment the results.
(h) Change $K_P$ to $100\mu A/V^2$, run the simulation and plot the drain current. Compare and comment the results.

The symbols in Fig. 4.1 show the transfer characteristic for $V_{T0} = 0V$ and $K_P = 20\mu A/V^2$. It is a straight line, originating at $V_{GS} = V_{T0} = 0V$, with the slope of $\frac{K_P}{L}V_{DS} = 0.033mA/V$. The change of $V_{T0}$ to $1V$ (the dashed line) shifts the transfer characteristic by $1V$ along the $V_{GS}$ axis, not affecting its slope. Note that the drain current is zero for gate voltages smaller than $V_{T0} = 1V$. The slope of the transfer characteristic is changed when $K_P$ is changed, as shown by
Vto, KP, L, and W

* Schematics Netlist *
M_M1 $N_{0002}$ $N_{0001}$ 0 $N_{0003}$ Mbreakn
+L=3u W=100u
V_VGS $N_{0001}$ 0 DC 0V
V_VDS $N_{0002}$ 0 DC 50mV
V_VSB 0 $N_{0003}$ DC 0

* Analysis Setup *
.DC LIN V_WGS 0 10 0.1

* Semiconductor Device Model *
.model Mbreakn NMOS (LEVEL=3
+ Vto=0 KP=20e-6)
+ Vto=1 KP=20e-6)
+ Vto=1 KP=100e-6)

Fig. 4.1 Exercise 4.1 (a)-(h)

the solid line. As the slope of the transfer characteristic is \( KP \frac{W}{L} V_{DS} \), it can also be changed by \( L \) and/or \( W \).

4.1.2 NMOS Inverter

Let us show the importance of properly setting \( L, W, V_{T0} \) and \( KP \) on the example of the simplest digital circuit, the inverter with resistive load (Section 4.2.2, Fig. 4.6 in the textbook). NMOS-
technology implementation of this inverter is shown in Fig. 5.11 of the textbook, where the resistor function is performed by the depletion-type MOSFET, while the switch function is performed by the enhancement type MOSFET. To simulate this circuit, it would be necessary to use N-channel MOSFETs with two different model names and two different sets of parameters. While this is possible in SPICE, the student version of PSPICE does not allow this option. Because of that, we will replace the switch from the generic circuit of Fig. 4.6 in the textbook by a MOSFET, and leave the resistor as is. The circuit obtained in this way is shown in Fig. 4.2.

Exercise 4.1

(i) Open/prepare the file of NMOS inverter, shown in Fig. 4.2.
(j) Set \( V_{\text{IN}}, V^+, \) and \( R_1 \) as in Fig. 4.2.
(k) Enable the DC analysis, and set the analysis parameters as in Fig. 4.2.
(l) Set \( L \) and \( W \) to 100\( \mu \)m each. Note that this are typically used default values of \( L \) and \( W \).
(m) Set the MOSFET parameters as follows: \( V_{T0} = 0 \) V and \( K_P = 20\mu A/V^2 \). These are the usual default values.
(n) Run the simulation and plot the output voltage. A good inverter should change the output voltage from high (\( \approx 5 \) V) to low (< 1 V) level. Set the y-axis range to 0–5. Record/print the results.
(o) Change \( L \) to 3\( \mu \)m, and repeat point (n). Compare and comment the results.

The symbols in Fig. 4.2 (a) and (b) show the results for \( L = 100\mu m \) and \( L = 3\mu m \) respectively. In the case of \( L = 100\mu m \) (the typical default value) the inverter does not behave as an inverter at all. The channel resistance of 100\( \mu \)m MOSFET is much larger than the load resistance (1k\( \Omega \)), and it causes a large voltage drop across it for both “off” and “on” states of the MOSFET. When the channel length is reduced to 3\( \mu \)m, the channel resistance is reduced 33 times, becoming much smaller than the load resistance when the MOSFET is in “on” state. Consequently, a small voltage drop appears across the MOSFET when it is in “on” state, while the voltage drop is still large when the MOSFET is in “off” state.

Exercise 4.1

(p) Change \( V_{T0} \) to 1V, run the simulation, and plot the output voltage. Compare and comment the results.
(q) Change \( K_P \) to 100\( \mu A/V^2 \), run the simulation, and plot the output voltage. Compare and comment the results.

The only change produced by the \( V_{T0} \) increase from 0 to 1V is a shift of the inverter characteristic along \( V_{\text{IN}} \) axis by 1V (dashed line versus symbols in Fig. 4.2 b). On the other hand, the increase of \( K_P \) leads to a smaller output voltage when the MOSFET is in “on” state, which is accompanied by a faster transition from “high” to “low” logic level at the output. These effects are due to reduced “on” resistance of the MOSFET.

4.2 Gamma and Phi

4.2.1 Linear Region - Nested Sweep

In the linear region, the effect of \( \gamma = \text{Gamma} \) and \( 2\phi_F = \Phi \) can be seen when non-zero source-to-bulk voltages are applied. A family of transfer characteristics, for different \( V_{SB} \) voltages, can be obtained by SPICE if \( V_{SB} \) is swept in addition to the \( V_{GS} \) sweeping, used to generate a
Vto, KP, L, and W

* Schematics Netlist *
M_Me $N0002 $N0001 0 0 Mbreakn
(a) +L=100u W=100u
(b) +L=3u W=100u
V_V+ $N0003 0 DC 5V
R_Rl $N0002 $N0003 1k
V_VIN $N0001 0

* Analysis Setup *
.DC LIN V_VIN 0 5 0.1

* Semiconductor Device Model *
.model Mbreakn NMOS (LEVEL=3
Vto=0 KP=20e-6)
Vto=1 KP=20e-6)
Vto=1 KP=100e-6)

Fig. 4.2 Exercise 4.1 (i)-(q)
single transfer characteristic. In SPICE, this is referred to as nested sweep. To set the parameters of a nested sweep in PSPICE, click on Nested Sweep inside the DC Sweep window, type the parameter values and click on Enable Nested Sweep. In the Analysis Setup command line, the parameters of the nested sweep are added after the parameters of the main sweep, as shown in Fig. 4.3.

Exercise 4.2
(a) Open the file of MOSFET biasing circuit, shown in Fig. 4.3.
(b) Check the values of L and W, and the values of the voltage sources VGS, VSB, and VDS.
(c) Enable and set the parameters of the main and the nested sweeps as in Fig. 4.3.
(d) Set the MOSFET parameters to VTO = 1V, KP = 100μA/V, and γ = 0.
(e) Run the simulation and plot the drain current (ID(M1)). Record/print the result.
(f) Change γ to 0.6V^{1/2} and set 2φF to 0.75V.
(g) Run the simulation and plot the drain current (ID(M1)). Compare and comment the results.

As the symbols in Fig. 4.3 show, no effect of VSB voltage is seen when γ = 0. The situation is completely different, however, for the case of γ = 0.6V^{1/2} and 2φF = 0.75V: the transfer characteristic is shifted along the VGS axis as VSB is increased. This is due to increase in the threshold voltage, which is known as the body effect.

4.2.2 Saturation Region
In the linear region, the body factor is important only for the case of non-zero VSB voltages. However, the situation is different in the saturation region where the body factor γ affects the characteristics even in the case of VSB = 0V. To see the effect of γ in the saturation region, let us generate the output MOSFET characteristics for zero and a non-zero value of γ.

Exercise 4.2
(h) Open the file of MOSFET biasing circuit, shown in Fig. 4.4.
(i) Check the values of L and W, and the values of the voltage sources VGS, VSB, and VDS.
(j) Enable and set the parameters of the main and the nested sweeps as in Fig. 4.4.
(k) Set the MOSFET parameters to VTO = 1V, KP = 100μA/V, and γ = 0.
(l) Run the simulation and plot the drain current (ID(M1)). Record/print the result.
(m) Change γ to 0.6V^{1/2} and set 2φF to 0.75V.
(n) Run the simulation and plot the drain current (ID(M1)). Compare and comment the results.

The results shown in Fig. 4.4 clearly show that γ reduces both the saturation current and the saturation voltage. This is in accordance with ID and VDSsat equations given in Tables A.4 and A.5, respectively (the dependence of ID and VDSsat in those equations is through the factor FB).

4.3 THETA
Mobility modulation constant θ = THETA is the most important second-order parameter, and its
Gamma and Phi

* Schematics Netlist *
M_M1 $N_0002 $N_0001 0 $N_0003 Mbreakn
+L=3u W=100u
V_VGS $N_0001 0 DC 0V
V_VDS $N_0002 0 DC 50mV
V_VSB 0 $N_0003 DC 0

* Analysis Setup *
.DC LIN V_VGS 0 5 0.1
+LIN V_VSB 0 5 1

* Semiconductor Device Model *
.model Mbreakn NMOS (LEVEL=3 Vto=1 + KP=100e-6 Gamma=0)
.model Mbreakn NMOS (LEVEL=3 Vto=1 + KP=100e-6 Gamma=0.6 Phi=0.75)

Fig. 4.3 Exercise 4.2 (a)-(g).
**Gamma and Phi**

* Schematics Netlist *
M_M1 $N_0002$ $N_0001$ 0 $N_0003$ Mbreakn
+L=3u W=100u
V_VGS $N_0001$ 0 DC 0V
V_VDS $N_0002$ 0 DC 50mV
V_VSB 0 $N_0003$ DC 0

* Analysis Setup *
.DC LIN V_VDS 0 10 0.1
+LIN V_VGS 0 8 2

* Semiconductor Device Model *
.model Mbreakn NMOS (LEVEL=3 Vto=1
  + KP=100e-6 Gamma=0)
.model Mbreakn NMOS (LEVEL=3 Vto=1
  + KP=100e-6 Gamma=0.6 Phi=0.75)

**Fig. 4.4 Exercise 4.2. (h)-(n).**
effect will be shown on the transfer and output characteristics of a MOSFET, as well as on the performance of a CMOS inverter.

### 4.3.1 Transfer and Output Characteristics

**Exercise 4.3**

(a) Open the file of MOSFET biasing circuit, shown in Fig. 4.5.
(b) Check the values of $L$ and $W$, and the values of the voltage sources $V_{GS}$, $V_{SB}$, and $V_{DS}$.
(c) Enable DC analysis and set the parameters as in Fig. 4.5.
(d) Set the MOSFET parameters to $V_{T0} = 1V$, $KP = 100\mu A/V$, $\gamma = 0.6$, $2\phi_F = 0.75V$, and $\theta = 0$.
(e) Run the simulation and plot the drain current ($I_D(M1)$). Record/print the result.
(f) Change $\theta$ to $0.1V^{-1}$.
(g) Run the simulation and plot the drain current ($I_D(M1)$). Compare and comment the results.

The results shown in Fig. 4.5 clearly illustrate the significance of the current reduction caused by the mobility modulation constant $\theta$. This effect is discussed in detail in Section 5.3.4 of the textbook and the associated Fig. 5.20. The output characteristics, as in Fig. 5.20 (b), can also be calculated by SPICE:

**Exercise 4.3**

(h) Change the DC analysis setup, setting the parameters of the main and the nested sweeps as in Fig. 4.6.
(i) Change the value of $\theta$ back to 0.
(j) Run the simulation and plot the drain current ($I_D(M1)$). Record/print the result.
(k) Change $\theta$ again to $0.1V^{-1}$.
(l) Run the simulation and plot the drain current ($I_D(M1)$). Compare and comment the results.

### 4.3.2 CMOS Inverter

The CMOS technology is the most important digital IC technology, and the CMOS inverter (Fig. 5.14 in the textbook) is the simplest CMOS logic cell. Let us analyze the effect of $\theta$ on the performance of the CMOS inverter.
Exercise 4.3

(m) Open/prepare the file of CMOS inverter circuit, shown in Fig. 4.7.
(n) Set the channel lengths of both MOSFETs to 1\( \mu \)m, and the channel widths to 100\( \mu \)m and 200\( \mu \)m for the N-channel and P-channel MOSFETs, respectively. Set the loading capacitor \( C_l \) to 2\( pF \).
(o) Set \( V^+ \) to 3.3V, and the parameters of the input pulse voltage as in Fig. 4.7: high voltage level 3.3V, low voltage level 0V, delay time 1ns, rise and fall times 0.1ns each, pulse width 5ns, period 10ns.
(p) Enable the transient analysis, and set the analysis parameters as in Fig. 4.7.
(q) Set the MOSFET parameters as in Fig. 4.7 (N-channel MOSFET: \( V_{T0} = 1.6V \), \( KP = 80\mu A/V^2 \), \( \gamma = 0.70V^{1/2} \), \( 2\phi_F = 0.80V \), and \( \theta = 0 \); P-channel MOSFET: \( V_{T0} = -1.6V \), \( KP = 30\mu A/V^2 \), \( \gamma = 1.84V^{1/2} \), \( 2\phi_F = 0.88V \), and \( \theta = 0 \))
(r) Run the simulation and plot the output voltage. Record/print the result.
(s) Change \( \theta \) to 0.2\( V^{-1} \), for both MOSFETs, run the simulation and plot the output voltage. Compare and comment the results.
The simulation results are shown in Fig. 4.7. The effect of $\theta$ does not appear as dramatic as in the case of MOSFET characteristics. Nonetheless, the reduction of MOSFET currents leads to somewhat slower changes from one to the other logic state.
* Schematics Netlist *
M_breakn $N_0002 \ $N_0001 \ 0 \ 0 \ M_breakn
+ \ L=1u \ W=100u
M_breakp $N_0003 \ $N_0001 \ $N_0002 \ $N_0003
+ \ M_breakp \ L=1u \ W=200u
V_V+ $N_0003 \ 0 \ DC \ 3.3V
V_VIN $N_0001 \ 0 \ PULSE
+ \ 3.3V \ 0V \ 1ns \ 0.1ns \ 0.1ns \ 5ns \ 10ns
C_C1 \ 0 \ $N_0002 \ 2p

* Analysis Setup *
.tran 0.15ns 15ns

* Semiconductor Device Model *
.model M_breakn NMOS (LEVEL=3
+ \ Vto=1.6 \ KP=80u \ Gamma=0.70 \ Phi=0.80
+ \ THETA=0)
+ \ THETA=0.2)
.model M_breakp PMOS (LEVEL=3
+ \ Vto=-1.6 \ KP=30u \ Gamma=1.84 \ Phi=0.88
+ \ THETA=0)
+ \ THETA=0.2)

---

![Diagram of a MOSFET circuit with labels and connections]

Fig. 4.7 Exercise 4.3 (m)-(s).
4.4 ETA (MOS Amplifier)
As explained in Section 5.3.4 of the textbook (Fig. 5.21), the parameter $\eta = \text{ETA}$ is used to model the finite output resistance of MOSFETs. This effect is not as important in digital as in linear circuits. The generic circuit of a very common linear circuit (a voltage amplifier) is described in Section 4.1.3 of the textbook (Fig. 4.4). Replacing the voltage controlled current source by a MOSFET, a MOSFET amplifier is obtained. This circuit can be used to illustrate the effect of $\eta$ parameter.

4.4.1 Custom y-Axis Variables in PROBE
Voltages and currents can directly be selected as y-axis variables in SPICE. To plot gain, however, we need the ratio between two voltages and/or currents. PROBE accepts combinations of trace variables (voltages and currents) and mathematical operations. In PSPICE, this combination can be typed as Trace Command which appears in Add Traces window. In fact, it is only the symbols of mathematical operations that need to be typed, the voltages and currents appear in the Trace Command line when clicked on.

Exercise 4.4
(a) Open/prepare the file of MOS amplifier, shown in Fig. 4.8.
(b) Set $L$ and $W$ to 3\,$\mu$m and 100\,$\mu$m, respectively. Set the values of the resistors and capacitors as in Fig. 4.8. Set the DC voltage source $V_+$ to 12\,V, and the amplitude of the AC voltage source $V_s$ to 0.1\,V.
(c) Enable the AC analysis, and set the analysis parameters as in Fig. 4.8.
(d) Set the MOSFET parameters as follows: $V_{T0} = 0.35\,V$, $KP = 100\,\mu A/V^2$, $\gamma = 0.60V^{1/2}$, $2\phi_F = 0.75\,V$, $\theta = 0.1$, and $\eta = 0$.
(e) Run the simulation and plot the voltage gain. (To plot the gain, open Add Traces window and enter the following equation in the Trace Command line: $V(R1:2)/V(C1:1)$. Click OK.
(f) Change $\eta$ to 0.5, run the simulation and plot the voltage gain. Compare and comment the results.

The frequency response plot obtained by the AC analysis is shown in Fig. 4.8. A constant gain is observed for frequencies $> 100\,Hz$, with the actual gain depending on the parameter $\eta$. The ideal voltage controlled current source (infinite dynamic output resistance, that is $\eta = 0$) corresponds to the maximum achievable voltage gain (the dashed line in Fig. 4.8). Any reduction in the dynamic output resistance will cause a reduction in the gain, as the solid line in Fig. 4.8 shows.

The drop of the gain observed at low frequencies is a kind of high-pass filter action caused by the coupling capacitors $C_1$ and $C_2$. This simulation does not predict any gain drop at high frequencies, however, this is not realistic as shown in the following exercise.

4.5 $C_{gso}$, $C_{gdo}$, $C_{gbo}$
As mentioned many times, no simulation at high frequencies can be correct unless the parameters of the parasitic capacitances are properly set up. Let us see the effect of the components of the input MOSFET capacitance on the high-frequency response of the MOS amplifier. (The effect of the input capacitance on the high frequency performance of CMOS digital circuits will be analyzed in Section 6.1).
* Schematics Netlist *
M1 $N_0002 \ $N_0001 0 0 Mbreakn
+ L=3u W=100u
R1 $N_0001 \ $N_0003 470k
R2 0 $N_0001 100k
RD $N_0002 \ $N_0003 1k
R1 0 $N_0004 10k
C1 $N_0005 \ $N_0001 1uF
C2 $N_0002 \ $N_0004 1uF
V+ $N_0003 0 DC 12V
Vs $N_0005 0 AC 0.1V

* Analysis Setup *
.ac DEC 10 10 1G

* Semiconductor Device Model *
.model Mbreakn NMOS (LEVEL=3
+ Vto=0.35 KP=100e-6 Gamma=0.60
+ Phi=0.75 THETA=0.1
+ ETA=0)
+ ETA=0.5

---

**Fig. 4.8 Exercise 4.4.**
4.5.1 MOS Amplifier

Exercise 4.5

(a) Open the file of MOS amplifier, shown in Fig. 4.9.
(b) Check $L$ and $W$, the values of the resistors and capacitors, and the parameters of the voltage sources.
(c) Make sure that the AC analysis is enabled, and set the analysis parameters as in Fig. 4.9.
(d) Keep the MOSFET parameters as in Exercise 4.4, making sure that $\eta = 0.5$, and add the following parameters: $C_{GS0} = 0$, $C_{GD0} = 0$, and $C_{GB0} = 0$.
(e) Run the simulation and plot the voltage gain. Record/print the result.
(f) Change the capacitance parameters to: $C_{GS0} = 1.4nF/m$, $C_{GD0} = 1.4nF/m$ and $C_{GB0} = 140nF/m$. Run the simulation and plot the voltage gain. Compare and comment the results.

Setting the capacitance parameters to zero (the symbols in Fig. 3.9) does not change anything, as the default values used in Exercise 4.4 are equal to zero anyway. However, the frequency response plot changes when realistic values of the capacitance parameters are set (the solid line). There is a gain drop for frequencies higher than 300 MHz, which is due to a low-pass filter action of the input MOSFET capacitance.
Fig. 4.9 Exercise 4.5 (a)-(f).
The computer exercises from this section illustrate the most important BJT SPICE parameters.

5.1 IS

A simple biasing circuit, like the one shown in Fig. 5.1, can be used to obtain BJT characteristics with SPICE. Note that a current source rather than a voltage source is connected to the BJT input (either the input current $I_B$ or the input voltage $V_{BE}$ can be used when expressing BJT characteristics.

Exercise 5.1

(a) Open/prepare the file of BJT biasing circuit, shown in Fig. 5.1.
(b) Set $V_{CE}$ to 5V to ensure that the BJT is in the active region. For a start, set $I_B$ to zero.
(c) Enable the DC analysis, and set the analysis parameters as in Fig. 5.1.
(d) Set $I_S0$ to 1pA.
(e) Run the simulation and plot the collector current ($I_C-Q1$). This gives $I_C-I_B$ plot. Record/print the result. To obtain the $I_C-V_{BE}$ characteristic by PROBE, $V(IB:-)$ has to be selected as X-axis variable. To do this in PSPICE, click on Plot, X Axis Settings..., Axis Variable..., and then click on $V(IB:-)$ to select it. This will show a linear $I_C-V_{BE}$ plot. To obtain a log-linear plot, like the ones used in Section 6.4 of the textbook, click on Plot, Y Axis Settings..., and then select Log inside the Y Axis Settings window. Record/print the results.
(f) Change $I_S0$ to 10pA, run the simulation and plot $I_C-I_B$ and $I_C-V_{BE}$ characteristics again. Compare and comment the results.

As Fig. 5.1 shows, the parameter $I_{S0} = IS$ does not affect the $I_C-I_B$ dependence. This is because $I_{S0}$ does not affect the slope of the $I_C-I_B$ characteristic, which is set by another and independent parameter ($\beta_F$). Similarly to the case of P-N junction diode, the parameter $I_{S0}$ determines the turn-on voltage: a smaller $V_{BE}$ voltage corresponds to the same $I_B$ (and therefore $I_C$) when $I_{S0}$ is larger. This is obvious from the linear-linear $I_C-V_{BE}$ plot shown in Fig. 5.1. It is worthwhile mentioning that the slope of this characteristic (that is obviously different at different $V_{BE}$ voltages) is the transconductance, which is a frequently used small-signal parameter as explained in Section 4.1.2 of the textbook. The log–linear $I_C–V_{BE}$ plots show the straight lines familiar from the parameter measurement graphs (for example, Fig. 6.30 in the textbook).
* Schematics Netlist *
Q_Q1 $N_0002 $N_0001 0 Qbreakn
V_VCE $N_0003 0 DC 5V
I_IB 0 $N_0001 DC 0A

* Analysis Setup *
.DC DEC I_IB 0 10mA 2.5mA

* Semiconductor Device Model *
.model Qbreakn NPN (IS=1pA)
.model Qbreakn NPN (IS=10pA)

Fig. 5.1 Exercise 5.1.
5.2 BF

5.2.1 Transfer Characteristics

Let us use the same circuit, the same analysis set up, and the same type of graphs to see the effects of $\beta_F$ parameter.

Exercise 5.2

(a) Open the file of BJT biasing circuit, shown in Fig. 5.2.
(b) Check the settings of the voltage sources and the DC analysis.
(c) Set the BJT parameters as follows: $I_{S0} = 1pA$, and $\beta_F = 100$ (this is a typical default value).
(d) Run the simulation and plot the different forms of transfer characteristics, as in Exercise 5.1. Record/print the results.
(e) Change $\beta_F$ to 200, run the simulation and plot the transfer characteristics again. Compare and comment the results.

Obviously, the slope of $I_C$-$I_B$ characteristic doubles when the value of $\beta_F$ is doubled. The parameter $\beta_F$, however, does not affect the $I_C$-$V_{BE}$ characteristic. This should not be surprising as, basically, $I_C = I_S(e^{V_{BE}/V_t} - 1)$ (refer to the $I_C$ equation of Table A.9).

5.2.2 Output Characteristics

Nested loops can be used to obtain transistor output characteristics by SPICE. Let us see the effect of $\beta_F$ on the BJT output characteristics.

Exercise 5.2

(f) Open the file of BJT biasing circuit, and change the DC analysis settings to correspond to the Analysis Setup line of Fig. 5.3.
(g) Set the BJT parameters as follows: $I_{S0} = 1pA$, and $\beta_F = 100$.
(h) Run the simulation and plot the collector current. Record/print the results.
(i) Change $\beta_F$ to 200, run the simulation and plot the collector current. Compare and comment the results.

The results (given in Fig. 5.3) show that the collector current, for any input base current, doubles when the current gain $\beta_F$ is doubled.

5.2.3 BJT Amplifier

A BJT can be used in the voltage amplifier circuit of Fig. 4.4 in the textbook. It is interesting to see the effects of the BJT current gain ($\beta_F$) on the voltage gain of this amplifier.

Exercise 5.2

(j) Open/prepare the file of BJT amplifier, shown in Fig. 5.4.
(k) Set the values of the voltage sources, the resistors and capacitors as in Fig. 5.4.
(l) Enable the transient analysis, and set the analysis parameters as in Fig. 5.4.
(m) Set the BJT parameters as follows: $I_{S0} = 1pA$, and $\beta_F = 100$.
(n) Run the simulation and plot the output voltage. Record/print the result.
(o) Change $\beta_F$ to 200, and repeat step (n).
(p) Change $\beta_F$ to 400, and repeat step (n). Compare and comment the results.

The increase of $\beta_F$ from 100 to 200 shows that the voltage gain is increased as well. However, the voltage gain increase has a limit, as the example of $\beta_F = 400$ (the solid line in Fig. 5.4)
* Schematics Netlist *
Q1 $N_{0002}$ $N_{0001}$ Qbreakn
V_{VCE} $N_{0003}$ 0 DC 5V
I_{IB} 0 $N_{0001}$ DC 0A

* Analysis Setup *
.DC DEC I_{IB} 0 10mA 2.5mA

* Semiconductor Device Model *
.model Qbreakn NPN (IS=1pA + BF=100)
 + BF=200)

*BJT*

\[ IB(Q1) \quad (mA) \]
\[ IC(Q1) \quad (A) \]
\[ V @ \text{node 1} \quad (V) \]

\[ \text{slope} = B \]
\[ \text{slope} = g_m \]

\[ \text{Fig. 5.2 Exercise 5.2 (a)-(e).} \]
shows. In this case, the output voltage is distorted, because the operating point is pushed out of the active region of BJT operation (if necessary, refer to Fig. 4.4 in the textbook, and the text of Section 4.1.3 for more detailed explanation).

5.3 VA

The Early voltage $V_A$ plays an analogous role to the parameter $\eta$ in the case of MOSFETs: it determines the value of the dynamic output resistance of the BJT. The effect of this parameter on
* Schematics Netlist *
Q1 $N_{0002}$ $N_{0001}$ 0 Qbreakn
RRC $N_{0002}$ $N_{0003}$ 4.7k
R2 0 $N_{0001}$ 10k
R1 $N_{0001}$ $N_{0003}$ 150k
C $N_{0002}$ $N_{0004}$ 1u
C1 $N_{0005}$ $N_{0001}$ 1u
VCC $N_{0003}$ 0 DC 10V
Rl 0 $N_{0004}$ 10k
Vs $N_{0005}$ 0
+SIN 0V 0.01V 1kHz 0 0 0

* Analysis Setup *
.tran 0.05ms 2.5ms

* Semiconductor Device Model *
.model Qbreakn NPN (IS=1pA
+ BF=100)
+ BF=200)
+ BF=400)

Fig. 5.4 Exercise 5.2 (j)-(p).
the output BJT characteristics is illustrated in Figs. 6.25 and 6.31 in the textbook. This exercise is analogous to Exercise 4.5 (Fig. 4.8).

**Exercise 5.3**

(a) Open the file of BJT amplifier (Fig. 5.5), and change the settings of the input voltage source $V_S$ so to prepare it for AC analysis: (1) the parameter $V_{\text{ampl}}$ (the second number in the SIN row of the Schematics Netlist) is a transient-analysis related parameter and it should be set to zero; (2) the amplitude of the input signal for the purpose of AC analysis is set by the $\text{AC}$ parameter of the $v\text{oltage source}$ (set to 0.01V, this adds $AC$ 0.01V in the $V_{\text{Vs}}$ line of the Schematic Netlist).

(b) Set the BJT parameters as follows: $I_{S0} = 1pA$, and $\beta_F = 200$ (as $V_A$ is ignored the default value $V_A = \infty$ will be taken by SPICE).

(c) Run the simulation and plot the gain (Exercise 4.4 describes how to plot combinations of trace variables). Record/print the results.

(d) Set $V_A$ to 20V, run the simulation and plot the gain. Compare and comment the results.

Similarly to the results obtained for the MOSFET amplifier, the finite output resistance of the BJT causes gain reduction.

**5.4 ISE and IKF**

SPICE BJT model is presented in two levels, Ebers-Moll level (Table A.9) and Gummel-Poon level (Table A.10). The Gummel-Poon level is automatically activated when $C_2I_{S0} = ISE$ and/or $I_{KF} = IKF$ (or the analogous inverse active mode parameters $C_4I_{S0} = ISC$ and/or $I_{KR} = IKR$) are specified. As the Gummel-Poon level in SPICE is about the current gain variation, let us see the influence of these parameters on the frequently presented, bell-shaped $\beta_F-I_C$ dependence.

**Exercise 5.4**

(a) Open the file of BJT biasing circuit, and set the DC analysis parameters as in Fig. 5.6.

(b) Set the BJT parameters as follows: $I_{S0} = 1pA$, and $\beta_F = 200$ (this is the Ebers-Moll level as neither $C_2I_{SE}$ nor $I_{KF}$ are specified).

(c) Run the simulation and plot the BJT current gain versus the collector current, using Log scale for the $I_C$ axis (Exercise 4.4 describes how to plot combinations of trace variables, while Exercise 5.1 describes how to set custom X axis and Log scale). Record/print the results.

(d) Set $C_2I_{S0}$ to 0.5pA, and repeat step (c).

(e) Set $I_{KF}$ to 0.1A, and repeat step (c). Compare and comment the results.

The results show that the current gain is constant for the case of the Ebers-Moll level (the dashed line in Fig. 5.6). When a non-zero value is specified for $C_2I_{S0}$, a “leakage” component is added to the base current (refer to the $I_B$ equation in Table A.10). This reduces the current gain $\beta_F = I_C/I_B$, and does it more at lower $I_B$ (and therefore $I_C$) levels, because the leakage component is proportionally more pronounced at those levels (the symbols in Fig. 5.6). As the solid line in Fig. 5.6 shows, the parameter $I_{KF}$ causes $\beta_F$ reduction at high $I_C$ currents. This is due to the high-injection effects, described in Section 6.3.4 of the textbook.
* Schematics Netlist *
Q1 $N_0002$ $N_0001$ Qbreakn
R_RC $N_0002$ $N_0003$ 4.7k
R_R2 0 $N_0001$ 10k
R_R1 $N_0001$ $N_0003$ 150k
C_C2 $N_0002$ $N_0004$ 1u
C_C1 $N_0005$ $N_0001$ 1u
V_VCC $N_0003$ 0 DC 10V
R_R1 0 $N_0004$ 10k
V_Vs $N_0005$ 0 AC 0.01V
+SIN 0V 0.01V 1kHz 0 0 0

* Analysis Setup *
.ac DEC 10 10 1G

* Semiconductor Device Model *
.model Qbreakn NPN (IS=1pA BF=200
+ VA=20V)

---

Fig. 5.5 Exercise 5.3.
5.5 RE

There are quite a few BJT parameters related to various parasitic elements, $r_E = \text{RE}$ being one of them. This exercise illustrates the effect of $r_E$ on the $I_C-V_{BE}$ characteristics, examined previously in Exercises 5.1 and 5.2.
Exercise 5.5

(a) If the BJT biasing circuit, used in the previous exercise is still open, and you have the results of the previous simulation, run PROBE and plot the log-linear $I_C-V_{BE}$ characteristic, as shown in Fig. 5.7 (the symbols). If not, open the BJT biasing-circuit file, run the simulation making sure that the parameters are as in Fig. 5.7 (the symbols), and then plot the log-linear $I_C-V_{BE}$ characteristic. (Ignoring the $r_E$ parameter means that the default zero value is taken.) Record/print the results.

(b) Set $r_E$ to 1Ω, run the simulation and plot the log-linear $I_C-V_{BE}$ characteristic. Compare and comment the results.

In Exercises 5.1 and 5.2 (no values for $I_{KF}$ and $r_E$ were specified), linear log $I_C-V_{BE}$ dependencies were observed throughout the whole $I_C$ range. When the $I_{KF}$ parameter is specified, a smaller $I_C$ current is obtained at high injection levels, leading to some deviation of the log $I_C-V_{BE}$ from the linear dependence (the symbols in Fig. 5.7). However, the effect of $I_{KF}$ on the log $I_C-V_{BE}$ characteristic is much smaller compared to the effect caused by the parasitic emitter resistance $r_E$ (the solid line in Fig. 5.7). This is because $r_E I_E$ voltage drop adds to the ideal $V_{BE}$ voltage, where the emitter current is $(β_F + 1)$ times larger than $I_B$.

5.6 CJE, VJE, MJE, CJC, VJC, and MJC

Similarly to the case of MOSFETs (Exercise 4.5), no proper high-frequency simulation can be performed unless the parameters of the parasitic capacitances are properly specified. Therefore, the perfect high-frequency response of the BJT amplifier, shown in Fig. 5.5, is not actually real. The parasitic capacitances in BJTs are mainly due to the two P–N junctions (base-emitter and base-collector), the depletion-layer capacitances of those P–N junctions being modeled by the same equations and analogous parameters as in the case of diodes. The effects of the parasitic capacitances on the frequency response of a BJT amplifier are illustrated in this exercise, analogously to the MOSFET amplifier illustrated in Exercise 4.5.

Exercise 5.6

(a) Open the file of BJT amplifier (Fig. 5.8), and make sure that the settings of the input voltage source and the AC analysis are as in Fig. 5.8.

(b) Set the BJT parameters as follows: $I_{S0} = 1pA$, and $β_F = 200$, $V_A = 20V$, $C_{2I_{S0}} = 0.5pA$, and $I_{KF} = 0.1A$. To begin with, ignore the parameters of parasitic BJT capacitances.

(c) Run the simulation and plot the gain. Record/print the results.

(d) Add the depletion-layer capacitance parameters for both junctions, using the following values: $C_{dE}(0) = 3pF$, $V_{biE} = 0.85V$, $m_E = 0.45$, $C_{dC}(0) = 3pF$, $V_{biC} = 0.70V$, and $m_C = 0.35$.

(e) Run the simulation and plot the gain. Compare and comment the results.

As expected, the low-pass filter effect of the parasitic capacitances causes gain drop at frequencies higher than $10MHz$. This is much lower frequency compared to the case of MOSFET amplifier (Fig. 4.9), however, it should be noted that the maximum mid-range gain is much larger in the case of the BJT amplifier.

There is stored-charge capacitance, in addition to the depletion-layer capacitance. There would be some charge stored at the forward-biased base-emitter P–N junction, however, the base-emitter
bias changes only slightly when the BJT operates in the amplifier circuit. Consequently, there is no need for stored charge accumulation and removal, and the stored-charge effects do not significantly influence the frequency response of the BJT amplifier.

5.7 TF

As opposed to the BJT amplifier considered in the previous exercise, the stored-charge effects are very important when the BJT is used as a switch.
* Schematics Netlist *
Q1 $N_0002$ $N_0001$ 0 Qbreakn
R1 $N_0002$ $N_0003$ 4.7k
R2 0 $N_0001$ 10k
R1 $N_0001$ $N_0003$ 150k
C1 $N_0002$ $N_0004$ 1u
C2 $N_0005$ $N_0001$ 1u
VCC $N_0003$ 0 DC 10V
R1 0 $N_0004$ 10k
Vs $N_0005$ 0 AC 0.01V
+SIN 0V 0.01V 1kHz 0 0 0

* Analysis Setup *
.ac DEC 10 10 1G

* Semiconductor Device Model *
.model Qbreakn NPN (IS=1pA BF=200
+ VA=20 ISE=0.5pA IKF=0.1A

+ CJE=3pF VJE=0.85V MJE=0.45
+ CJC=3pF VJC=0.70V MJC=0.35)

---

Fig. 5.8 Exercise 5.6.
Exercise 5.7

(a) Open/prepare the file of BJT switch circuit, shown in Fig. 5.9.
(b) Set the parameters of the voltage sources and the resistors as in Fig. 5.9.
(c) Enable the transient analysis, and set the analysis parameters as in Fig. 5.9.
(d) Set the BJT parameters as follows: $I_{S0} = 1\, \mu A$, $\beta = 200$, $C_{dE}(0) = 0.3\, \text{nF}$, $V_{BE} = 0.75\, \text{V}$, $m_E = 0.40$, $C_{dC}(0) = 0.3\, \text{nF}$, $V_{BC} = 0.65\, \text{V}$, and $m_C = 0.33$. To begin with, ignore $\tau_F$, which is by default set to zero.
(e) Run the simulation and plot the input and output voltages. Record/print the results.
(f) Set $\tau_F$ to 10\,\text{ns}, run the simulation, and plot the output voltage. Compare and comment the results.

When the parameter $\tau_F$ is not specified (by default $\tau_F = 0$), the switch works perfectly at 1\,MHz, as the dashed line in Fig. 5.9 shows. However, the simulation with $\tau_F = 0$ ignores the stored-charge effect. When the BJT is operated as a closed switch (low output voltage), both the base-emitter and the base-collector junctions are in saturation. This causes a significant minority-carrier charge storage at the junctions, in particular the base-emitter junction that conducts a significant current. When the input voltage is suddenly changed, the BJT cannot turn off before the stored charge is drained through the input resistor $R_{in}$. Similarly, the BJT cannot be turned on immediately as it takes some time to accumulate the steady-state level of the stored charge. These effects are obvious from the simulation results performed with $\tau_F = 10\,\text{ns}$ (the solid line in Fig. 5.9). More detailed discussion about the stored charge effect and the transit time is provided in sub-section 3.2.2 of the textbook.
Fig. 5.9 Exercise 5.7.
6
ADVANCED DEVICES

6.1 CMOS Down-Scaling

The load capacitance $C_l$ in the CMOS circuits used in Exercise 4.3 (m)-(s) (Fig. 4.7) represents the input capacitances of the logic gates connected to the output of the inverter. As we wish to perform a more realistic study of the effects of the input capacitance, it is useful to replace the load capacitor by a single CMOS inverter connected to the output of the first CMOS inverter (therefore, we have now a cascade connection of two identical CMOS inverters). Let us simulate this circuit at a high frequency (400 MHz), as implemented in a typical 1 $\mu$m CMOS technology.

Exercise 6.1

(a) Open/prepare the file of CMOS inverter, shown in Fig. 6.1.
(b) Set the channel lengths and widths of the MOSFETs, and the parameters of the voltage sources as in Fig. 6.1.
(c) Enable the transient analysis, and set the analysis parameters as in Fig. 6.1.
(d) Set the MOSFET parameters as in Fig. 6.1 (these parameters represent a typical 1 $\mu$m CMOS technology), with zero values for the input capacitance parameters (the dashed line).
(e) Run the simulation and plot the voltage at node 2 (the output of the first CMOS inverter). Record/print the result.
(f) Change the capacitance parameters to: $C_{GS} = 0.4 nF/m$, $C_{GD} = 0.4 nF/m$ and $C_{GB} = 170 nF/m$. Run the simulation and plot the voltage at node 2. Compare and comment the results.

Ignoring the capacitance parameters (the dashed line in Fig. 6.1), the simulation misleadingly shows almost perfect inverter operation even at as high frequency as 400 MHz. Much more realistic simulation is obtained when the capacitance parameters are included (the solid line in Fig. 6.1). The distortion that is obvious in this case is due to the fact that the currents of MOSFETs $M_3/M_1$ are too small to quickly enough charge/discharge the relatively large input capacitances of MOSFETs $M_2$ and $M_4$.

Down-scaling of MOSFET dimensions can significantly improve the speed of CMOS ICs. To illustrate this effect, let us reduce the channel length and width of the MOSFETs by factor of $S = 4$. Section 7.1.2 of the textbook describes that such a channel length reduction is practically meaningful only if the other device parameters are appropriately adjusted to avoid possible adverse effects. Let us apply the simplest down-scaling rules, saying that the substrate doping
Cgso, Cgdo, and Cgbo

* Schematics Netlist *
M_M1 $N_0002 $N_0001 0 0 Mbreakn + L=1u W=100u
M_M2 $N_0003 $N_0002 0 0 MbreakN + L=1u W=100u
M_M3 $N_0004 $N_0001 $N_0002 + $N_0004 MbreakL L=1u W=200u
M_M4 $N_0004 $N_0002 $N_0003 + $N_0004 MbreakP L=1u W=200u
V_V+ $N_0004 0 DC 3.3V
V_Vp $N_0001 0 PULSE 3.3V 0V + 0.1ns 0.1ns 0.1ns 1.25ns 2.5ns

* Analysis Setup *
.tran 0.04ns 4ns

* Semiconductor Device Model *
.model Mbreakn NMOS (LEVEL=3 + Vto=1.60 KP=80e-6 + Gamma=0.70 Phi=0.80 THETA=0.2 + Cgso=0 Cgdo=0 Cgbo=0)
.model Mbreakp PMOS (LEVEL=3 + Vto=-1.60 KP=30e-6 + Gamma=1.84 Phi=0.88 THETA=0.2 + Cgso=0 Cgdo=0 Cgbo=0)
.model Mbreakp PMOS (LEVEL=3 + Vto=-1.60 KP=30e-6 + Gamma=1.84 Phi=0.88 THETA=0.2 + Cgso=0 Cgdo=0 Cgbo=0)
.model Mbreakp PMOS (LEVEL=3 + Vto=-1.60 KP=30e-6 + Gamma=1.84 Phi=0.88 THETA=0.2 + Cgso=0 Cgdo=0 Cgbo=0)

Fig. 6.1 Exercise 6.1 (a)-(f).
should be increased $S^2$ times\(^1\), and the gate oxide thickness should be reduced $S$ times\(^2\). Applying these rules, the MOSFET parameters can be recalculated to represent a 0.25\(\mu\)m CMOS technology.

Exercise 6.1

(g) To simulate the CMOS inverter as implemented in 0.25\(\mu\)m CMOS technology, set the MOSFET parameters as in Fig. 6.2. To begin with, use zero values for the input capacitance parameters (the dashed line).

(h) Run the simulation and plot the voltage at node 2 (the output of the first CMOS inverter). Record/print the result.

(i) Change the capacitance parameters to: $C_{GS0} = 0.4nF/m$, $C_{GD0} = 0.4nF/m$ and $C_{GB0} = 340nF/m$. Run the simulation and plot the voltage at node 2. Compare and comment the results.

As the results show (Fig. 6.2), the inverter works properly even at 400 MHz with the 0.25\(\mu\)m MOSFETs. This is because the dimension down scaling reduced the input capacitances and at the same time increased the currents, cutting dramatically down the times needed to charge and discharge the input capacitance when the logic state is being changed.

\(^1\)As the depletion layer width of an abrupt P–N junction is inversely proportional to $\sqrt{N_{A,B}}$ (refer to Eqs. 2.33 and 2.34 in the textbook), this ensures a proportional reduction of the depletion layer width to avoid punch-through.

\(^2\)The gate oxide reduction is necessary to avoid the undesirable threshold voltage increase due to the concentration increase (refer to the third term of Eq. 2.75 in the textbook)
Cgso, Cgdo, and Cgbo – down scaling

* Schematics Netlist *
M_M1 $N_0002 $N_0001 0 0 Mbreakn
  + L=0.25u W=25u
M_M2 $N_0003 $N_0002 0 0 MbreakN
  + L=0.25u W=25u
M_M3 $N_0004 $N_0001 $N_0002
  + $N_0004 Mbreakp L=0.25u W=50u
M_M4 $N_0004 $N_0002 $N_0003
  + $N_0004 MbreakP L=0.25u W=50u
V_V+ $N_0004 0 DC 3.3V
V_Vp $N_0001 0 PULSE 3.3V 0V
  + 0.1ns 0.1ns 0.1ns 1.25ns 2.5ns

* Analysis Setup *
.tran 0.04ns 4ns

* Semiconductor Device Model *
.model Mbreakn NMOS (LEVEL=3
  + Vto=1.70 KP=160e-6
  + Gamma=0.70 Phi=0.94 THETA=0.2
  + Cgso=0 Cgdo=0 Cgbo=0)
      + Cgso=0.4n Cgdo=0.4n Cgbo=170n)
.model Mbreakp PMOS (LEVEL=3
  + Vto=-1.88 KP=60e-6
  + Gamma=1.84 Phi=1.04 THETA=0.2
  + Cgso=0 Cgdo=0 Cgbo=0)
      + Cgso=0.4n Cgdo=0.4n Cgbo=340n)

Fig. 6.2 Exercise 6.1 (g)-(i).
7

PHOTONIC DEVICES

7.1 LED
Although SPICE cannot handle things like the light intensity, color, etc. of LEDs, circuits involving LEDs may need to be simulated by SPICE. In this exercise, SPICE is used to analyze the effect of the resistance $R$ in the LED driver circuit of Fig. 8.1 in the textbook.

7.1.1 DC Analysis - Sweeping a Component Value
It is possible to sweep a resistor value in SPICE in order to analyze its effect on the circuit performance. This appears as an additional type of DC analysis. To enable this, the following steps are necessary:

1. The value of the resistor has to be set as a parameter. The second line in the Schematics Netlist, given in Fig. 7.1, shows that this is achieved by using a variable resistor name, typed inside curly brackets: {...}. This is in contrast to simply setting/typing the component value, for example 1k. In PSPICE, this is done by a double click on the component value, and then changing the component value to $<\text{var}>$, where $<\text{var}>$ can be anything that you want to use as the variable resistor name.

2. The variable component values need to be defined as parameters, as shown by the line 
   .PARAM RVAR=1k in Fig. 7.1. In PSPICE, subsequent clicks on Draw, Get New Part, Browse, special.slb (inside Library), PARAM (inside Part), OK, followed by positioning and a click will place PARAMETERS: legend as shown in the circuit diagram of Fig. 7.1. A double click on Parameters: will open a window where the variable resistor name (NAME1=) can be typed (no curly brackets). The nominal resistor value has to be typed inside the same window (VALUE1=). The nominal resistor value is only needed for the original bias point calculation that SPICE performs. In the case shown in Fig. 7.1, NAME1=RVAR, and VALUE1=1k.

3. Finally, the word PARAM, followed by the parameter name (variable resistor name), has to appear in the .DC command line used to set up the sweep parameters. The .DC command line shown in Fig. 7.1 means that the resistor value will be swept from 400Ω to 2kΩ, in steps of 100Ω. The DC sweep parameters are set in PSPICE in the usual way: clicks on Analysis, Setup, and DC Sweep open the DC Sweep window where Global Parameter is selected, and Start Value, End Value and Increment are typed.
Exercise 7.1

(a) Open/prepare the file of LED driver circuit shown in Fig. 7.1.
(b) Set the value of V1 to 5V.
(c) Change the resistor value to a parameter name (RVAR), insert and open the parameter legend (PARAMETERS:), and type the resistor details, as shown in Fig. 7.1.
(d) Enable the DC analysis, and set the analysis parameters as in Fig. 7.1.
(e) Set the diode parameters as follows: $I_S = 10^{-12}$ and $n = 1$. These parameters represent a silicon diode (rectifier).
(f) Run the simulation, plot the current through the diode, and comment the results. Print/record the diode current.
(g) Change the $I_S$ parameter to $10^{-40}$, to account for the higher “turn-on” voltage encountered in LEDs (Exercises 3.1 and 3.2 deal with the relationship between the “turn-on” voltage and $I_S$ parameter).
(h) Run the simulation and plot the diode current again. Compare and comment the results.
The current flowing through the diode is proportional to the light intensity. The nominal and/or maximum operating current is specified for any particular type of LED, although it is typically in the order of several mA. Obviously, a smaller resistance corresponds to a larger current. However, the important thing here is the difference between the silicon rectifier diode (the circles in the graph of Fig. 7.1) and the LED (the solid line). If the desired current is 6mA, 750Ω resistor is needed in the case of the silicon diode. If a similar value of the $I_S$ parameter was used for the LED in this circuit, the circuit would be designed with $R_1 \approx 750\Omega$, which would actually result with a current smaller than 4mA. The solid line in Fig. 7.1 shows that a 470Ω resistor would be needed to achieve $\approx 6mA$ of current through the LED.

7.2 Photodetector Diode

As SPICE cannot accept light intensity as a circuit excitation, the photodetector diode is modeled as a diode in parallel with a current source representing the photocurrent. A PSPICE diagram of the photodetector circuit discussed in Section 8.2.1 of the textbook (Fig. 8.6) is given in Fig. 7.2.

Exercise 7.2

(a) Open/prepare the file of photodetector circuit shown in Fig. 7.2.
(b) Set the value of $I_{\text{photo}}$, $V_R$ and $R$, as in Fig. 7.2.
(c) Enable the DC analysis, and set the parameters so as to sweep $I_{\text{photo}}$ from 0 to 80mA in steps of 1mA.
(d) Set the diode parameters as follows: $I_S = 10^{-12}$ and $n = 1$.
(e) Run the simulation, plot the output voltage, and comment the results.

For a proper operation of the photodetector circuit, the diode should be reverse biased. In the reverse-bias region, the photodiode acts as a light-controlled current source, pushing a light-intensity dependent current through the resistor R, which converts the current into output voltage. Consequently, the output voltage linearly increases with the light intensity. The simulation results plotted in Fig. 7.2 show this type of circuit response up to about 45mA of $I_{\text{photo}}$. When the photocurrent is increased further, the output voltage is pinned at about 7.5V. The reason for this is the fact that the output voltage cannot be increased beyond $V_R + V_D$, where $V_D$ is the forward-bias voltage of the diode. In the range of photocurrents higher than $\approx 45mA$, the photodiode is in “on” mode, and the increased photocurrent flows through the diode rather than through the resistor.

Exercise 7.2

(f) Change $I_S$ to $10^{-30}$A.
(g) Run the simulation, plot the output voltage, compare and comment the results.

The only noticeable effect of the change of $I_S$ from $10^{-12}$A to $10^{-30}$A is the increase of the forward-bias voltage ($V_D$), as discussed in Exercises 3.1, 3.2 and 7.1. The $I_S$ increase is unimportant compared to the photocurrent, and it does not have a noticeable effect on the circuit response when the diode is properly reverse biased. The increase in $V_D$ however, does increase the photocurrent threshold that turns the diode “on”, as it increases the maximum possible output voltage $V_R + V_D$. 
7.3 Solar Cell

The basic solar-cell circuit (Fig. 8.7 in the textbook) can also be analyzed by SPICE if the solar cell is replaced by a current source connected in parallel to a diode. The power taken from the solar cell depends on the load resistance. It is interesting to analyze this dependence by SPICE simulation. To do this, the load resistance has to be swept, which can be done as explained in Exercise 7.1. In addition, power rather than voltage or current is needed as the output variable.
Exercise 7.3

(a) Open/prepare the file of solar cell circuit shown in Fig. 7.3.
(b) Set the value of $I_{\text{photo}}$, and diode parameters as in Fig. 7.3.
(c) Set the resistor value as a parameter (the procedure is described in Exercise 7.1).
(d) Enable the DC analysis, and set the parameters so as to sweep $R$ from 1Ω to 50Ω in steps of 0.5Ω.
(e) Run the simulation.
(f) Plot the output current, the output voltage and the output power. You may wish to use different PROBE windows for the three different graphs: current, voltage and power. (Exercise 4.4 describes how to plot combinations of trace variables.)
(g) Comment the results.

The results (Fig. 7.3) show that almost the complete photocurrent (40mA) flows through the load when the load resistance is small. However, the output voltage is also small in this case, leading to a small delivered power. As the load resistance is increased, the output voltage is increased as well, increasing the power. However, the increase in the output voltage increases the current through $D_1$, and when this current becomes significant, the current flowing through the load resistor is significantly reduced. The voltage cannot increase much when the diode is in “on” mode, and the output power decreases as the current is reduced by increase in the load resistance. In this example, load resistance of about 12Ω extracts maximum power from the solar cell.
Solar Cell

* Schematics Netlist *
I_Iphoto 0 $N_0001 DC 40mA
D_D1 $N_0001 0 Dbreak
R_Rload $N_0001 0 {R}

* Analysis Setup *
.PARAM R=10
.DC LIN PARAM R 1 50 0.5

* Semiconductor Device Model *
.model Dbreak D(IS=1e-10A N=1)

Fig. 7.3 Exercise 7.3
8

POWER DEVICES

8.1 MOSFET Switch

A frequent issue with the power MOSFETs is the proper gate driving (switch control). This exercise shows the importance of the parasitic gate resistance, in addition to the input capacitance, for proper simulation of MOS switching circuits. As the simplest case of a resistive load is considered in this example, the circuit becomes structurally identical to the NMOS inverter considered in Section 4. In reality, all sorts of loads are used, the inductive loads being especially frequent.

Exercise 8.1

(a) Open/prepare the file of MOS switch circuit, shown in Fig. 8.1.
(b) Set $L$ and $W$ to $3\mu m$ and $0.3\mu m$, respectively. Set the values of the resistor and the parameters of the voltage sources as in Fig. 8.1.
(c) Enable the transient analysis, and set the analysis parameters as in Fig. 8.1.
(d) Set the MOSFET parameters as follows: $V_T = 2.8V$, $K_P = 20\mu A/V^2$, $\gamma = 0.708V^{1/2}$, $\varphi_F = 0.608V$, $\theta = 0$, $\eta = 0$, $C_{GS0} = 9nF/m$, $C_{GD0} = 1.7nF/m$ (these parameters represent a typical power MOSFET; no separate $C_{GB0}$ parameter is needed as the source and bulk are short-circuited), and to begin with $R_G = 0$.
(e) Run the simulation and plot the output voltage. Record/print the result.
(f) Change $R_G$ to $14\Omega$, run the simulation and plot the output voltage. Compare and comment the results.

With $R_G = 0$, the circuit works almost perfectly, as the output voltage levels are reached fairly quickly (the dashed line in Fig. 8.1). However, with $R_G = 14\Omega$ the time constant of the input circuit becomes significant, causing a significant delay and a relatively soft switching from one state to the other. Also, note that a significant gate current (as high as $0.5A$) is needed to turn the MOSFET on and off.
* Schematics Netlist *
M_Msw $N_{0002}$ $N_{0001}$ 0 0 Mbreakn
+ L=2u W=0.3
R_Rl $N_{0002}$ $N_{0003}$ 5
V_V+ $N_{0003}$ 0 DC 10V
V_Vs $N_{0001}$ 0 DC 3 PULSE
+ 10V 0V 10ns 1ns 1ns 100ns 200ns

* Analysis Setup *
.tran 1ns 300ns

* Semiconductor Device Model *
.model Mbreakn NMOS (LEVEL=3 Vto=2.8
+ KP=20e-6 gamma=0.70 Phi=0.60
+ theta=0 eta=0 Cgso=9n Cgdo=1.7n
+ Rg=0)
+ Rg=14)

---

Fig. 8.1 Exercise 8.1.
### A

#### Tables of Device Parameters and Equations

Table A.1 Summary of the SPICE diode model: Static I-V characteristic

<table>
<thead>
<tr>
<th>Symbol</th>
<th>SPICE Keyword</th>
<th>Parameter Name</th>
<th>Typical Value/Range</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_S$</td>
<td>$IS$</td>
<td>Saturation current</td>
<td>$1 - 2$</td>
<td>A</td>
</tr>
<tr>
<td>$n$</td>
<td>$N$</td>
<td>Emission coefficient</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$r_S$</td>
<td>$RS$</td>
<td>Parasitic resistance</td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>$BV$</td>
<td>$BV$</td>
<td>Breakdown voltage (positive number)</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$IBV$</td>
<td></td>
<td>Breakdown current (positive number)</td>
<td></td>
<td>A</td>
</tr>
</tbody>
</table>

Note: $IBV = IS \frac{BV}{V_t}$

#### STATIC DIODE MODEL

$$I_D(V_{D0}) = \begin{cases} 
  IS \left( e^{\frac{V_{D0}}{V_t}} - 1 \right) + V_{D0}G_{MIN} & \text{if } V_{D0} > -BV \\
  -IBV & \text{if } V_{D0} = -BV \\
  -IS \left[ e^{\left( \frac{BV + V_{D0}}{V_t} \right)} - 1 + \frac{BV}{V_t} \right] & \text{if } V_{D0} < -BV
\end{cases}$$
Table A.2  Summary of the SPICE diode model: Dynamic characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>SPICE Keyword</th>
<th>Parameter Name</th>
<th>Typical Value/ Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_d(0)$</td>
<td>CJ0</td>
<td>Zero-bias junction capacitance</td>
<td>$F$</td>
</tr>
<tr>
<td>$V_{bi}$</td>
<td>VJ</td>
<td>Built-in (junction) voltage</td>
<td>0.65 – 1.25 $V$</td>
</tr>
<tr>
<td>$m$</td>
<td>M</td>
<td>Grading coefficient</td>
<td>$\frac{1}{3} - \frac{1}{2}$ $V$</td>
</tr>
<tr>
<td>$\tau_T$</td>
<td>TT</td>
<td>Transit time</td>
<td>$s$</td>
</tr>
</tbody>
</table>

LARGE-SIGNAL DIODE MODEL

$I_D(V_{D0})$ is given in Table A.1

$C_D = C_d + C_s$

$C_d = CJ0 \left(1 - \frac{V_{D0}}{V_J}\right)^{-M}$ (for $V_{D0} < 0.5V_J$)

$C_s = TT \left. \frac{dI_D}{dV_{D0}} \right|$
Table A.3 Summary of the SPICE diode model: Temperature effects

<table>
<thead>
<tr>
<th>Symbol</th>
<th>SPICE Keyword</th>
<th>Parameter Name</th>
<th>Typical Value/ Range</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E_g$</td>
<td>EG</td>
<td>Energy gap</td>
<td>1.12 for Si</td>
<td>eV</td>
</tr>
<tr>
<td>$p_t$</td>
<td>XTI</td>
<td>Saturation current temperature</td>
<td>3</td>
<td></td>
</tr>
</tbody>
</table>

**TEMPERATURE-DEPENDENT DIODE MODEL**

**Static Characteristic**

$$I_S(T) = I_S \left( \frac{T}{T_{nom}} \right)^{XTI} \times \exp \left[ - \frac{q E_g}{kT} \left( 1 - \frac{T}{T_{nom}} \right) \right]$$

**Dynamic Characteristics**

$$V_{bi}(T) \approx \frac{T}{T_{nom}} V_J - 2 \frac{kT}{q} \ln \left( \frac{T}{T_{nom}} \right)^{1.5}$$

$$C_d(0, T) = C_{JO} \left\{ 1 + M \left[ 400 \times 10^{-6} (T - T_{nom}) - \frac{V_{bi}(T) - V_J}{V_J} \right] \right\}$$

**NOTE:** $I_S$, $V_J$ and $C_{JO}$ express the values of these parameters at the nominal temperature $T_{nom}$ as stated in Table A.1, and Table A.2
Table A.4 Summary of SPICE LEVEL-3 static MOSFET model

**GEOMETRICAL VARIABLES**

\[ L_{\text{eff}} = L_g - 2x_{\text{lat}} \quad (x_{\text{lat}} \text{ is a parameter; refer to Table 5.5}) \]

<table>
<thead>
<tr>
<th>Symbol</th>
<th>SPICE Keyword</th>
<th>Variable Name</th>
<th>Default Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( L_g )</td>
<td>L</td>
<td>Gate length</td>
<td>100 ( \times 10^{-6} )</td>
<td>m</td>
</tr>
<tr>
<td>( W )</td>
<td>W</td>
<td>Channel width</td>
<td>100 ( \times 10^{-6} )</td>
<td>m</td>
</tr>
</tbody>
</table>

NOTE: \( L \) and \( W \) can also be specified as parameters

**STATIC LEVEL-3 MODEL**

\[
I_D = \begin{cases} 
\beta[(V_{GS} - V_T)V_{DS} - (1 + F_B)\frac{V_{DS}^2}{2}], & \text{triode region} \\
\frac{\beta}{2(1+F_B)}(V_{GS} - V_T)^2, & \text{satur. region} \quad (1)
\end{cases}
\]

\[
V_{\text{subth}} = V_{TS} - V_{GS} \geq 0
\]

\[
F_B = \frac{\gamma F_s}{2\sqrt{|2\phi_F|+V_{SB}}} + F_n \quad (2)
\]

\[
\beta, V_{DS\text{sat}}, V_T, |2\phi_F|, \gamma, F_s, F_n, n_s
\]

<table>
<thead>
<tr>
<th>Principal Effects</th>
<th>Second-Order Effects</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel Layer</td>
<td>Table A.5 Table A.6</td>
</tr>
<tr>
<td>Related Related</td>
<td>Table A.5 Table A.6</td>
</tr>
<tr>
<td>All</td>
<td>Table A.5 Table A.6</td>
</tr>
</tbody>
</table>

\( V_{\text{max}} \) is not specified.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>SPICE Keyword</th>
<th>Parameter Name</th>
<th>Typical Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$KP$</td>
<td>KP</td>
<td>Transconductance</td>
<td>$1.2 \times 10^{-4}$</td>
<td>$A/V^2$</td>
</tr>
<tr>
<td>$\mu_0$</td>
<td>Uo</td>
<td>Low-field mobility †</td>
<td>700</td>
<td>$cm^2/Vs$</td>
</tr>
<tr>
<td>$t_{ox}$</td>
<td>Tox</td>
<td>Gate-oxide thickness †</td>
<td>$20 \times 10^{-9}$</td>
<td>$m$</td>
</tr>
<tr>
<td>$V_{T0}$</td>
<td>Vto</td>
<td>Zero-bias threshold</td>
<td>1</td>
<td>$V$</td>
</tr>
<tr>
<td>$</td>
<td>2\phi_F</td>
<td>$</td>
<td>Phi</td>
<td>Surface potential in strong inversion</td>
</tr>
<tr>
<td>$\gamma$</td>
<td>Gamma</td>
<td>Body-effect parameter</td>
<td>$&gt;0.3$</td>
<td>$V^{1/2}$</td>
</tr>
</tbody>
</table>

**EQUATIONS**

**NMOS**

$$\beta = \begin{cases} KP \frac{W}{L_{eff}}, & \text{if } KP \text{ is specified} \\ \mu_0 \frac{W}{L_{ox}} \frac{W}{L_{eff}}, & \text{if } KP \text{ is not specified} \end{cases}$$

$$L_{\text{pinch}} = 0 \quad (\text{KAPPA}=0)$$

$$V_T = V_{T0} + \text{Gamma} \left( \sqrt{\phi_1 + V_{SB}} - \sqrt{\phi_1} \right)$$

$$V_{DSSat} = \frac{V_{GS} - V_T}{1 + F_s}$$

$$F_s = 1 \quad (\text{Xj}=0)$$

$$F_n = 0 \quad (\text{DELTA}=0)$$

$$n_s = 1 + \frac{\gamma F_s (\Phi_1 + |V_{SB}|)^{-1/2}}{2} \quad (\text{NFS}=0)$$

**PMOS**

$$\beta = V_{T0} - \text{Gamma} \left( \sqrt{\phi_1 + V_{BS}} - \sqrt{\phi_1} \right)$$

**CONSTANT:** $\varepsilon_{ox} = 3.9 \times 8.85 \times 10^{-12} F/m$

* and † indicate incompatible parameters
Table A.6 Summary of SPICE LEVEL 3 static parameters: Channel related second-order effects

<table>
<thead>
<tr>
<th>CHANNEL RELATED STATIC PARAMETERS</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Symbol</td>
<td>SPICE Keyword</td>
<td>Parameter Name</td>
</tr>
<tr>
<td>$KP$ (or $KP^{*}$)</td>
<td>$KP$</td>
<td>Transconductance</td>
</tr>
<tr>
<td>$\mu_0$ and $U_0$</td>
<td>$t_{ox}$</td>
<td>Low-field mobility $^{†}$</td>
</tr>
<tr>
<td>$\theta$</td>
<td>$\Theta$</td>
<td>Gate-oxide thickness $^{†}$</td>
</tr>
<tr>
<td>$v_{\text{max}}$</td>
<td>$V_{\text{max}}$</td>
<td>Mobility modulation constant</td>
</tr>
<tr>
<td>$\kappa$</td>
<td>$\kappa$</td>
<td>Maximum drift velocity</td>
</tr>
<tr>
<td>$N_A, N_D$</td>
<td>$N_{\text{sub}}$</td>
<td>Channel length modulation coefficient (needs $N_{\text{sub}}$)</td>
</tr>
</tbody>
</table>

$\beta$ and $V_{DS\text{sat}}$ EQUATIONS

\[
\beta = \frac{\mu_{\text{eff}} \varepsilon_{\text{ox}}}{t_{\text{ox}} L_{\text{eff}} - L_{\text{pinch}}} \\
\mu_{\text{eff}} = \frac{\mu_{0}}{1 + \mu_{s} \min(|V_{DS}|, |V_{DS\text{sat}}|)/(V_{\text{max}} L_{\text{eff}})} \\
\mu_{s} = \frac{\mu_{0}}{1 + \Theta |V_{GS} - V_{T}|} \\
\mu_{0} = KP \frac{t_{\text{ox}}}{\mu_{s}}, \text{ if } KP \text{ is specified; else } \mu_{0} = U_0 \\
L_{\text{pinch}} = \left\{ \begin{array}{ll}
L_a = \sqrt{\frac{\kappa \varepsilon_{\text{ox}} 2}{q N_{\text{sub}}}} |V_{DS} - V_{DS\text{sat}}|, & \text{if } V_{\text{max}} \text{ is not specified} \\
\left[ \left( \frac{\varepsilon_{\text{ox}} V_{DS\text{sat}}}{q N_{\text{sub}} L_{\text{eff}}} \right)^2 + L_a^2 \right]^{1/2} - \frac{\varepsilon_{\text{ox}} |V_{DS\text{sat}}|}{q N_{\text{sub}} L_{\text{eff}}}, & \text{if } V_{\text{max}} \text{ is specified}
\end{array} \right.
\]

\[
V_{DS\text{sat}} = \left\{ \begin{array}{ll}
\frac{V_{GS} - V_{T}}{1 + F_{B}}, & \text{if } V_{\text{max}} \text{ is not specified} \\
V_{DS\text{sat} - corr}, & \text{if } V_{\text{max}} \text{ is specified}
\end{array} \right.
\]

\[
V_{DS\text{sat} - corr} = V_a + V_b - \sqrt{V_a^2 + V_b^2} \quad (2) \\
V_{DS\text{sat} - corr} = V_a - V_b + \sqrt{V_a^2 + V_b^2} \quad (2)
\]

\[
V_a = \frac{V_{GS} - V_{T}}{1 + F_{B}}, \quad V_b = \frac{V_{\text{max}} L_{\text{eff}}}{\mu_{s}} \quad (2)
\]

CONSTANT: $\varepsilon_{\text{ox}} = 3.9 \times 8.85 \times 10^{-12} F/m$

$^{*}$ and $^{†}$ indicate incompatible parameters


Table A.7  Summary of SPICE LEVEL 3 static parameters: Depletion-layer related second-order effects

<table>
<thead>
<tr>
<th>Symbol</th>
<th>SPICE Keyword</th>
<th>Parameter Name</th>
<th>Typical Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{ox}$</td>
<td>Tox</td>
<td>Gate oxide thickness</td>
<td>$20 \times 10^{-9}$</td>
<td>$m$</td>
</tr>
<tr>
<td>$\eta$</td>
<td>ETA</td>
<td>Static feedback</td>
<td>0.7</td>
<td>-</td>
</tr>
<tr>
<td>$N_A, N_D$</td>
<td>$N_{sub}$</td>
<td>Substrate doping concentration</td>
<td>$10^{15}$</td>
<td>$cm^{-3}$</td>
</tr>
<tr>
<td>$N_{oc}$</td>
<td>$N_{ss}$</td>
<td>Oxide-charge density (needs $N_{sub}$)</td>
<td>$10^{10}$</td>
<td>$cm^{-2}$</td>
</tr>
</tbody>
</table>
| TPG | - same as drain/source: TPG = 1  
- opposite of D/S: TPG = -1  
- Al: TPG=0 | Gate material type (needs $N_{sub}$) | - | |
| $x_j$ | Xj | P-N junction depth (needs $N_{sub}$) | $0.5 \times 10^{-6}$ | $m$ |
| $x_{j-lat}$ | Ld | Lateral diffusion | $0.8 \times x_j$ | $m$ |
| $V_{bi}$ | PB | P-N junction built-in voltage (needs $N_{sub}$) | 0.8 | $V$ |
| $\delta$ | DELTA | Width effect on threshold voltage | 1.0 | - |
| NFS | | Subthreshold-current fitting parameter | $10^{11}$ | $cm^{-2}$ |
Table A.7 Summary of SPICE LEVEL 3 static parameters: Depletion-layer related second-order effects – PART II

| NMOS | \( V_T, 2|\phi_F|, \gamma, F_s, F_n, \) and \( n_s \) | EQUATIONS |
|------|---------------------------------|------------|
| \( C_{ox} = \varepsilon_{ox}/\Tox \) | \( \Rightarrow V_T = V_{T0} + \gamma F_s \left( \sqrt{2|\phi_F| + V_{SB}} - \sqrt{2|\phi_F|} \right) - \sigma_D V_{DS} + F_n(V_{SB} + 2\phi_F) \) | \( V_T = V_{T0} - \gamma F_s \left( \sqrt{2|\phi_F| + V_{BS}} - \sqrt{2|\phi_F|} \right) - \sigma_D V_{DS} - F_n(V_{BS} + 2|\phi_F|) \) |
| \( V_{T0} = \phi_{ms} - \frac{q N_{SS}}{\varepsilon_{ox}} + 2|\phi_F| + \gamma F_s \sqrt{2|\phi_F|} \) | \( \Rightarrow \phi_{ms} = \begin{cases} -\frac{E_s}{2q} - |\phi_F|, & \text{if TPG} = 1 \\ \frac{F_s}{2q} - |\phi_F|, & \text{if TPG} = -1 \\ \phi_s - |\phi_F|, & \text{if TPG} = 0 \end{cases} \) | \( \Rightarrow \phi_{ms} = \begin{cases} \frac{E_s}{2q} + |\phi_F|, & \text{if TPG} = 1 \\ \frac{F_s}{2q} + |\phi_F|, & \text{if TPG} = -1 \\ \phi_s + |\phi_F|, & \text{if TPG} = 0 \end{cases} \) |

\( \sigma_D = 8.15 \times 10^{-22}\varepsilon/(C_{ox} L_{eff}^3) \) \(^{(1)}\)

| \( \Rightarrow \gamma = \frac{1}{C_{ox}} \sqrt{2\varepsilon_s q N_{sub}} \) | \( \Rightarrow |2\phi_F| = 2 \frac{kT}{q} \ln \frac{N_{sub}}{n_i} \) |

\( F_s = 1 - \frac{\chi_j}{L_{eff}} \left( \frac{L_{d} + w_p}{\chi_j} \sqrt{1 - \frac{w_p}{x_j + w_p} - \frac{L_{d}}{x_j}} \right) \) \(^{(1)}\)

\( w_p = \sqrt{\frac{2\varepsilon_s}{q N_{sub}} \left( PB + V_{SB} \right)} \) \( w_p = \sqrt{\frac{2\varepsilon_s}{q N_{sub}} \left( PB + V_{BS} \right)} \)

\( w_c = 0.06313353 \chi_j + 0.8013929 w_p - 0.0111077 \frac{w_p^2}{\chi_j} \) \(^{(1)}\)

| \( \Rightarrow F_n = \Delta \varepsilon / \left( 4C_{ox} W \right) \) \(^{(1)}\) | \( \Rightarrow n_s = 1 + \frac{q N_{SS}}{C_{ox}} + \frac{\gamma F_s (2|\phi_F| + |V_{SB}|)^{-1/2} - F_n}{2} \) \(^{(2)}\) |

CONSTANTS:
\( \varepsilon_{ox} = 3.45 \times 10^{-11} F/m \) \( k = 8.62 \times 10^{-5} eV/K \) \( n_i = 1.4 \times 10^{10} \text{cm}^{-3} \)
\( q = 1.6 \times 10^{-19} C \) \( \phi_s = \phi_m - 4.61 V \) \( \varepsilon_s = 1.044 \times 10^{-10} F/m \)


### GEOMETRICAL VARIABLES

<table>
<thead>
<tr>
<th>Symbol</th>
<th>SPICE Keyword</th>
<th>Variable Name</th>
<th>Default Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A_D$; $P_D$</td>
<td>$AD$; $PD$</td>
<td>Drain diffusion area; ... perimeter</td>
<td>0; 0</td>
<td>$m^2$; $m$</td>
</tr>
<tr>
<td>$A_S$; $P_S$</td>
<td>$AS$; $PS$</td>
<td>Source diffusion area; ... perimeter</td>
<td>0; 0</td>
<td>$m^2$; $m$</td>
</tr>
</tbody>
</table>

### PARASITIC-ELEMENT RELATED PARAMETERS

<table>
<thead>
<tr>
<th>Related</th>
<th>Symbol</th>
<th>SPICE Keyword</th>
<th>Parasitic Element</th>
<th>Parameter Name</th>
<th>Typical Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{ox}$</td>
<td>$Tox$</td>
<td>$C_{S1}; C_{D1}$</td>
<td>Gate oxide thickness</td>
<td>$20 \times 10^{-9}$</td>
<td>$m$</td>
<td></td>
</tr>
<tr>
<td>$[2\phi_F]$ (or $N_{A,D}$)</td>
<td>$Phi$ (or $N_{sub}$)</td>
<td>$C_{S1}$; $C_{D1}$</td>
<td>Surface potential (substrate doping)</td>
<td>$(10^{15})$</td>
<td>$(cm^{-3})$</td>
<td></td>
</tr>
<tr>
<td>$C_{GDO}$</td>
<td>$Cgdo$</td>
<td>$C_{D2}$</td>
<td>Gate–drain overlap capacitance per channel width</td>
<td>$4 \times 10^{-11}$</td>
<td>$F/m$</td>
<td></td>
</tr>
<tr>
<td>$C_{GS0}$</td>
<td>$Cgso$</td>
<td>$C_{S2}$</td>
<td>Gate-source overlap capacitance per channel width</td>
<td>$4 \times 10^{-11}$</td>
<td>$F/m$</td>
<td></td>
</tr>
<tr>
<td>$C_{GB0}$</td>
<td>$Cgbo$</td>
<td>not shown</td>
<td>Gate–bulk overlap capacitance per channel length</td>
<td>$2 \times 10^{-10}$</td>
<td>$F/m$</td>
<td></td>
</tr>
<tr>
<td>$I_S$ (or $J_S$)</td>
<td>$IS$ (or $JS$)</td>
<td>$D_B$</td>
<td>Saturation current (... current density)</td>
<td>$10^{-14}$</td>
<td>$A$</td>
<td></td>
</tr>
<tr>
<td>$V_{bi}$</td>
<td>$PB$/$PBSW$</td>
<td>$D_B/D_P$</td>
<td>Built-in voltage</td>
<td>0.8</td>
<td>$V$</td>
<td></td>
</tr>
<tr>
<td>$C_d(0)$</td>
<td>$Cj$/$Cjsw$</td>
<td>$D_B/D_P$</td>
<td>zero-bias capacitance per unit area/length</td>
<td>$2 \times 10^{-4}$; $10^{-9}$</td>
<td>$F/m^2$/</td>
<td></td>
</tr>
<tr>
<td>$m$</td>
<td>$Mj$/$Mjsw$</td>
<td>$D_B/D_P$</td>
<td>Grading coefficient (incompatible with $V_{bi}$, $C_d(0)$, and $m$)</td>
<td>$\frac{1}{3}$; $\frac{1}{2}$</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>$C_{BD}$; $C_{BS}$</td>
<td>$Cbd$; $Cbs$</td>
<td>$D_B/D_P$</td>
<td>Drain/source-to-bulk capacitance</td>
<td>$F$</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Table A.8  Summary of SPICE dynamic MOSFET model – PART II

LARGE-SIGNAL EQUIVALENT CIRCUIT

<table>
<thead>
<tr>
<th>ID(V\textsubscript{GS},V\textsubscript{DS},V\textsubscript{SB})</th>
<th>RD</th>
<th>DBDB</th>
<th>DPDP</th>
</tr>
</thead>
<tbody>
<tr>
<td>RS</td>
<td>CS\textsubscript{2}</td>
<td>Cs1</td>
<td>CD1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>CD2</td>
</tr>
<tr>
<td>RG</td>
<td></td>
<td></td>
<td>RG</td>
</tr>
<tr>
<td>RB</td>
<td></td>
<td></td>
<td>RB</td>
</tr>
<tr>
<td>SD</td>
<td></td>
<td></td>
<td>SD</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>B</td>
</tr>
</tbody>
</table>

NOTE: Diodes shown for NMOS. Reverse for PMOS.

\( I_D(V_{GS},V_{DS},V_{SB}) \) is given in Table A.4
\( D_B/D_P \) - according to diode model of Table A.2
\( C_{S2} = C_{GS0}W \)
\( C_{D2} = C_{GD0}W \)
\( C_{GB} = C_{GB0}L_{\text{eff}}; C_{GB} \) appears between points 1 and 2 (not explicitly shown).
\( C_{S1} \) and \( C_{S2} \) calculated by SPICE from the terminal voltages, and \( t_{ox} \) and \( |2\phi_F| \) (or \( N_{A,D} \)) parameters
\( I_S = J_S A_D \) (drain-bulk)
\( I_S = J_S A_S \) (source-bulk)
Table A.9 Summary of SPICE BJT model: Static Ebers-Moll level

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Usual SPICE Keyword</th>
<th>Parameter Name</th>
<th>Typical Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{S0}$</td>
<td>IS</td>
<td>Saturation current</td>
<td>$10^{-16}$</td>
<td>A</td>
</tr>
<tr>
<td>$\beta_F$</td>
<td>BF</td>
<td>Normal c.e. current gain</td>
<td>150</td>
<td>-</td>
</tr>
<tr>
<td>$\beta_R$</td>
<td>BR</td>
<td>Inverse c.e. current gain</td>
<td>5</td>
<td>-</td>
</tr>
<tr>
<td>$V_A$</td>
<td>VA</td>
<td>Normal Early voltage</td>
<td>&gt; 50</td>
<td>V</td>
</tr>
<tr>
<td>$V_B$</td>
<td>VB</td>
<td>Inverse Early voltage</td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

**EBERS-MOLL MODEL**

**NPN BJT**

\[
I_S = IS (1 - \frac{V_{BC}}{V_{A}} - \frac{V_{EB}}{V_{B}}) \\
I_C = IS \left( e^{V_{BE}/V_t} - 1 \right) - \left( 1 + \frac{1}{\beta_R} \right) IS \left( e^{V_{BC}/V_t} - 1 \right) \\
I_E = -(1 + \frac{1}{\beta_F}) IS \left( e^{V_{BE}/V_t} - 1 \right) + IS \left( e^{V_{BC}/V_t} - 1 \right) \\
I_B = \frac{1}{\beta_F} IS \left( e^{V_{BE}/V_t} - 1 \right) + \frac{1}{\beta_F} IS \left( e^{V_{BC}/V_t} - 1 \right)
\]

**PNP BJT**

\[
I_S = IS (1 - \frac{V_{CB}}{V_{A}} - \frac{V_{EB}}{V_{B}}) \\
I_C = IS \left( e^{V_{EB}/V_t} - 1 \right) - \left( 1 + \frac{1}{\beta_R} \right) IS \left( e^{V_{CB}/V_t} - 1 \right) \\
I_E = -(1 + \frac{1}{\beta_F}) IS \left( e^{V_{EB}/V_t} - 1 \right) + IS \left( e^{V_{CB}/V_t} - 1 \right) \\
I_B = \frac{1}{\beta_F} IS \left( e^{V_{EB}/V_t} - 1 \right) + \frac{1}{\beta_F} IS \left( e^{V_{CB}/V_t} - 1 \right)
\]
Tables of Device Parameters and Equations

Table A.10 Summary of SPICE BJT model: Static Gummel-Poon level

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Usual SPICE Parameter Name</th>
<th>Typical Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{S0}$</td>
<td>$I_S$</td>
<td>Saturation current</td>
</tr>
<tr>
<td>$\beta_{FM}$</td>
<td>$BF$</td>
<td>Maximum normal current gain</td>
</tr>
<tr>
<td>$\beta_{RM}$</td>
<td>$BR$</td>
<td>Maximum inverse current gain</td>
</tr>
<tr>
<td>$V_A$</td>
<td>$VA$</td>
<td>Normal Early voltage</td>
</tr>
<tr>
<td>$V_B$</td>
<td>$VB$</td>
<td>Inverse Early voltage</td>
</tr>
<tr>
<td>$I_{KF}$</td>
<td>$IKF$</td>
<td>Normal knee current</td>
</tr>
<tr>
<td>$I_{KR}$</td>
<td>$IKR$</td>
<td>Inverse knee current</td>
</tr>
<tr>
<td>$C_2I_{S0}$</td>
<td>$I_{SE}$</td>
<td>B/E leakage saturation current</td>
</tr>
<tr>
<td>$n_{EL}$</td>
<td>$NE$</td>
<td>B/E leakage emission coefficient</td>
</tr>
<tr>
<td>$C_4I_{S0}$</td>
<td>$I_{SC}$</td>
<td>B/C leakage saturation current</td>
</tr>
<tr>
<td>$n_{CL}$</td>
<td>$NC$</td>
<td>B/C leakage emission coefficient</td>
</tr>
</tbody>
</table>

GUMMEL-POON MODEL

NPN BJT (equivalent circuit as in Table A.9)

$$
\lambda_{BE} = e^{\frac{V_{BE}}{V_i}} - 1 \\
\lambda_{BC} = e^{\frac{V_{BE} + V_{BC}}{V_i}} - 1 \\
q_1 = \left(1 - \frac{V_{BC}}{V_A} - \frac{V_{BE}}{V_B}\right)^{-1}, q_2 = \frac{IS_{BE}}{IKF} \lambda_{BE} + \frac{IS_{BC}}{IKR} \lambda_{BC}, \quad q_b = 0.5q_1 \left(1 + \sqrt{1 + 4q_2}\right)
$$

$$
I_B = \frac{IS_{BE}}{IB} \lambda_{BE} + I_{SE} \lambda_{BEL} + \frac{IS_{BC}}{IC} \lambda_{BC} + I_{SC} \lambda_{BCL}
$$

$$
I_E = -\frac{IS_{BE}}{Ib} (\lambda_{BE} - \lambda_{BC}) - \frac{IS_{BC}}{IC} \lambda_{BE} - I_{SE} \lambda_{BEL}
$$

PNP BJT (equivalent circuit as in Table A.9)

$$
\lambda_{EB} = e^{\frac{V_{EB}}{V_i}} - 1 \\
\lambda_{CB} = e^{\frac{V_{EB} + V_{CB}}{V_i}} - 1 \\
q_1 = \left(1 - \frac{V_{CB}}{V_A} - \frac{V_{EB}}{V_B}\right)^{-1}, q_2 = \frac{IS_{EB}}{IB} \lambda_{EB} + \frac{IS_{CB}}{IC} \lambda_{CB}, \quad q_b = 0.5q_1 \left(1 + \sqrt{1 + 4q_2}\right)
$$

$$
I_B = \frac{IS_{EB}}{IB} \lambda_{EB} + I_{SE} \lambda_{EBL} + \frac{IS_{CB}}{IC} \lambda_{CB} + I_{SC} \lambda_{CBL}
$$

$$
I_C = -\frac{IS_{EB}}{Ib} (\lambda_{EB} - \lambda_{CB}) - \frac{IS_{CB}}{IC} \lambda_{EB} - I_{SE} \lambda_{EBL}
$$

$$
I_E = -\frac{IS_{EB}}{Ib} (\lambda_{EB} - \lambda_{CB}) - \frac{IS_{CB}}{IC} \lambda_{EB} - I_{SE} \lambda_{EBL}
$$
Table A.11 Summary of SPICE BJT model: Parasitic elements

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Usual SPICE Keyword</th>
<th>Related Parasitic Element</th>
<th>Parameter Name</th>
<th>Typical Value/Range</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>r_B</td>
<td>RB</td>
<td>r_B</td>
<td>Base resistance</td>
<td>10</td>
<td>Ω</td>
</tr>
<tr>
<td>r_E</td>
<td>RE</td>
<td>r_E</td>
<td>Emitter resistance</td>
<td>2</td>
<td>Ω</td>
</tr>
<tr>
<td>r_C</td>
<td>RC</td>
<td>r_C</td>
<td>Collector resistance</td>
<td>15</td>
<td>Ω</td>
</tr>
<tr>
<td>C_{dE}(0)</td>
<td>CJE</td>
<td>C_{dE}</td>
<td>Zero-bias B/E capacitance</td>
<td>0.8</td>
<td>F</td>
</tr>
<tr>
<td>V_{biE}</td>
<td>VJE</td>
<td>C_{dE}</td>
<td>B/E built-in voltage</td>
<td>0.75</td>
<td>V</td>
</tr>
<tr>
<td>m_E</td>
<td>MJE</td>
<td>C_{dE}</td>
<td>B/E grading coefficient</td>
<td>1/2</td>
<td>−</td>
</tr>
<tr>
<td>τ_F</td>
<td>TF</td>
<td>C_sE</td>
<td>Normal transit time</td>
<td>10^{-3}</td>
<td>s</td>
</tr>
<tr>
<td>C_{dC}(0)</td>
<td>CJC</td>
<td>C_{dC}</td>
<td>Zero-bias B/C capacitance</td>
<td>F</td>
<td></td>
</tr>
<tr>
<td>V_{biC}</td>
<td>VJC</td>
<td>C_{dC}</td>
<td>B/C built-in voltage</td>
<td>0.75</td>
<td>V</td>
</tr>
<tr>
<td>m_C</td>
<td>MJC</td>
<td>C_{dC}</td>
<td>B/C grading coefficient</td>
<td>1/2</td>
<td>−</td>
</tr>
<tr>
<td>τ_R</td>
<td>TR</td>
<td>C_sC</td>
<td>Inverse transit time</td>
<td>10^{-9}</td>
<td>s</td>
</tr>
<tr>
<td>C_{dS}(0)</td>
<td>CJS</td>
<td>C_{dS}</td>
<td>Zero-bias C/S capacitance</td>
<td>F</td>
<td></td>
</tr>
<tr>
<td>V_{biS}</td>
<td>VJS</td>
<td>C_{dS}</td>
<td>C/S built-in voltage</td>
<td>0.7</td>
<td>V</td>
</tr>
<tr>
<td>m_S</td>
<td>MJS</td>
<td>C_{dS}</td>
<td>C/S grading coefficient</td>
<td>1/2</td>
<td>−</td>
</tr>
</tbody>
</table>

LARGE-SIGNAL EQUIVALENT CIRCUIT

NOTE: The diodes and the current-source direction are shown for NPN BJT. Reverse current direction and diode polarities apply in the case of PNP BJT.

\[
\begin{align*}
C_{dE} & \quad C_{dC} \\
C_{dS} & \quad C_sC \\
\end{align*}
\]

According to \( C_d \) equation of Table A.2

\[
\begin{align*}
C_{sE} & \quad C_{sC} \\
\end{align*}
\]

According to \( C_s \) equation of Table A.2